Principles, Design and Implementation of a Direct AC-to-AC Power Converter / Regulated Electronic Transformer

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**Abstract**

In the last three decades, technological developments reducing the dimensions and costs of electronic components have led to switching power converters taking the bulk of the energy conversion market. In principle, this market involves four types of conversion: DC–DC, DC–AC, AC–DC, and AC–AC. While the first three types are implemented directly in a single conversion, the fourth involves a dual AC–DC–AC conversion, requiring two serial converters. This article describes an innovative development of the first electronic transformer based on direct single-stage AC–AC conversion: a unique topology that combines high efficiency with the advantages of dual-stage power-quality protection. Our regulated electronic transformer is stabilized, controlled, and protected and can lock onto any line voltage (110 V or 220 V) with a frequency of 45 to 65 Hz. Stabilization is achieved via rapid pulse-width modulation technology, implemented via fast two-way solid-state switches; control is through a 150 MHz digital signal processor. The transformer has fully automatic digital protection against overcurrent and output short circuits. Our first-stage system is a single-phase device with 4 kW power in which the efficiency is better than 97% and the weight and volume are about one-tenth of an electromechanical transformer.

**Keywords**: AC–AC Converter; Electronic Transformer; Power Converting.

**1. Introduction**

Technological developments – in reducing the dimensions and costs of electronic components – have led to switching power converters taking the bulk of the energy conversion market. In principle, this market involves four types of converter: regulators (DC–DC), inverters (DC–AC), switching power supplies (AC–DC), and electronic transformers (AC–AC). While the first three of these are implemented directly in a single conversion, the fourth is implemented via a dual AC–DC–AC conversion, requiring a rechargeable battery and two serial converters (AC–DC and DC–AC).

Annual worldwide damage caused by voltage disturbances is estimated at billions of dollars: the worldwide economy is losing around 30 billion dollars a year to power-quality phenomena. Voltage fluctuations (sags, swells, surges, impulses, and harmonics) can result in considerable downtime and enormous expense as customers manually reset equipment and “clean up” disrupted manufacturing processes.

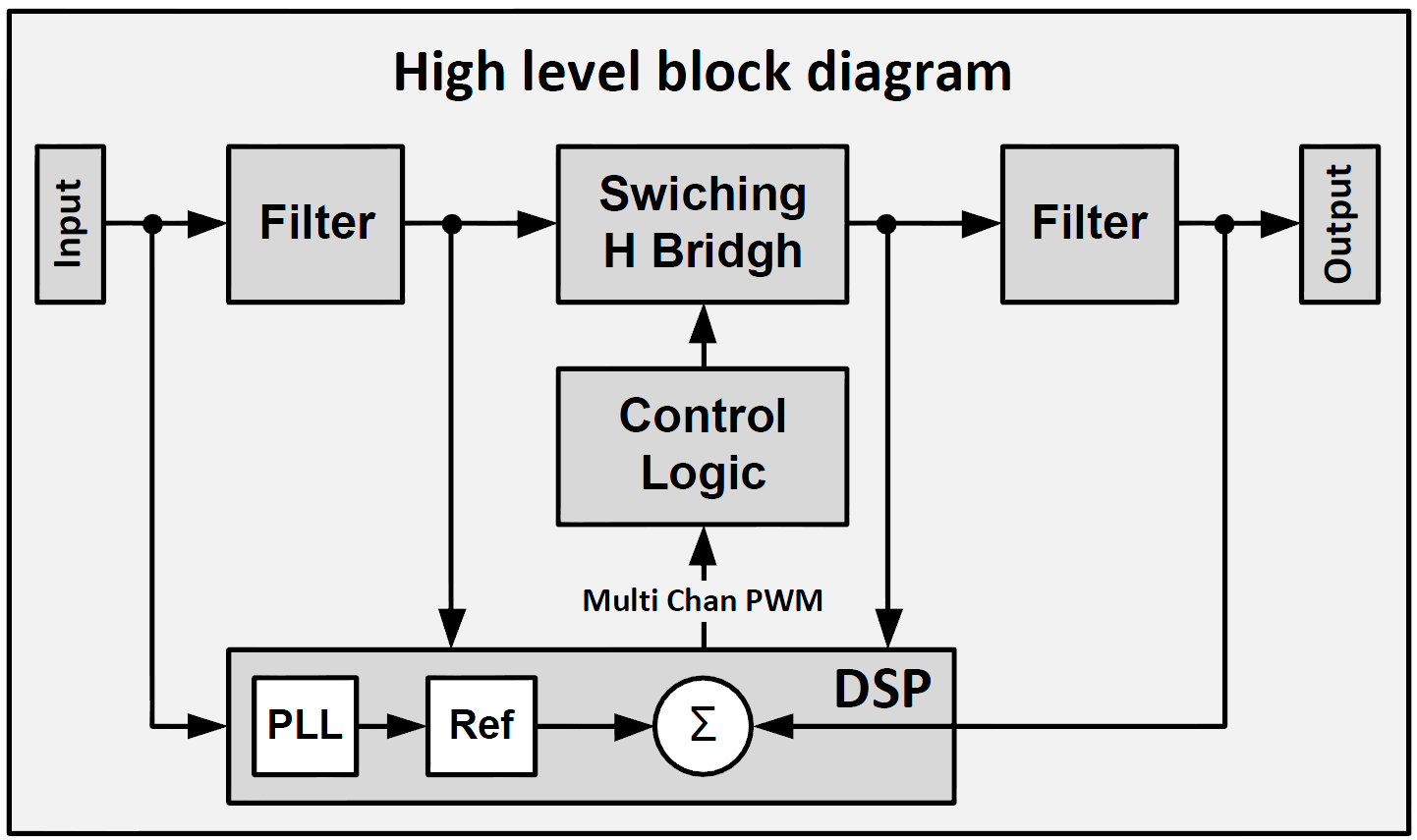
Over the past two decades, much work has been published on the subject of AC-to-AC conversion [1]– [20]. Although such articles have discussed single- or multi-phase conversion, and single- and two-stage conversion, none of them have demonstrated the real-time synthesis of alternating voltage from a pure reference waveform.

We were seeking to replace traditional, unreliable, and expensive electromechanical conversion technologies with compact, reliable, and accurate switching technology while staying “green” and cost-effective. Our regulated electronic transformer (RET) is a single-stage AC–AC converter that will herald a new era in AC conversion. It is optimal for power-quality conversion, energy mixing, and energy saving in industrial, commercial, and residential applications. It can replace the following: autotransformers; buck–boost transformers; ferroresonant transformers; all electromechanical regulators; uninterruptible power supplies (UPSs) where a backup is not needed. The RET converts AC input voltage while regulating AC output voltage with only a single conversion stage between them. We developed and built a single-phase 5 kW converter that demonstrates regulation with a conversion efficiency of 98%, a wide input voltage range of ±50 percent, and high power density, to illustrate the technology in which the weight and volume are about one-tenth of a traditional electromechanical transformer.

**2. System Architecture**

The building block of our RET is the equivalent of an autotransformer in which output voltage can vary in the range of 50–150% of input voltage with a response time of less than 100 μs. At the same time, the size and weight are significantly lower than standard switching converters. Applying a high-speed closed loop to such a switching transformer enables synthesis of a pure sinusoidal output waveform, independent of the input voltage waveform. Fig. 1 shows a high-level block diagram of our converter. The input voltage is fed into a filter and passes through a switching network, capable of step-up or step-down in relation to the voltage. The chopped voltage generated by the switches is then fed into an output filter to produce a clean output voltage. In addition, the input voltage is fed into a phase-locked loop (PLL) that is locked onto the input frequency and produces a pure mathematical reference of a sinusoidal (or other) waveform with which to compare the output voltage.

A real-time digital signal processor (DSP) is used to close the loop on the output voltage and keep it proportional to the reference voltage. The result is a pure sinusoidal output waveform, without any disturbances and free of harmonics. A stable output is maintained as long as the input voltage is within 50 to 150 percent of the desired output voltage, even if it is not a sinusoidal waveform; for example, it can be a square wave instead.



**Fig. 1.**

High-level block diagram of the direct AC–AC converter.

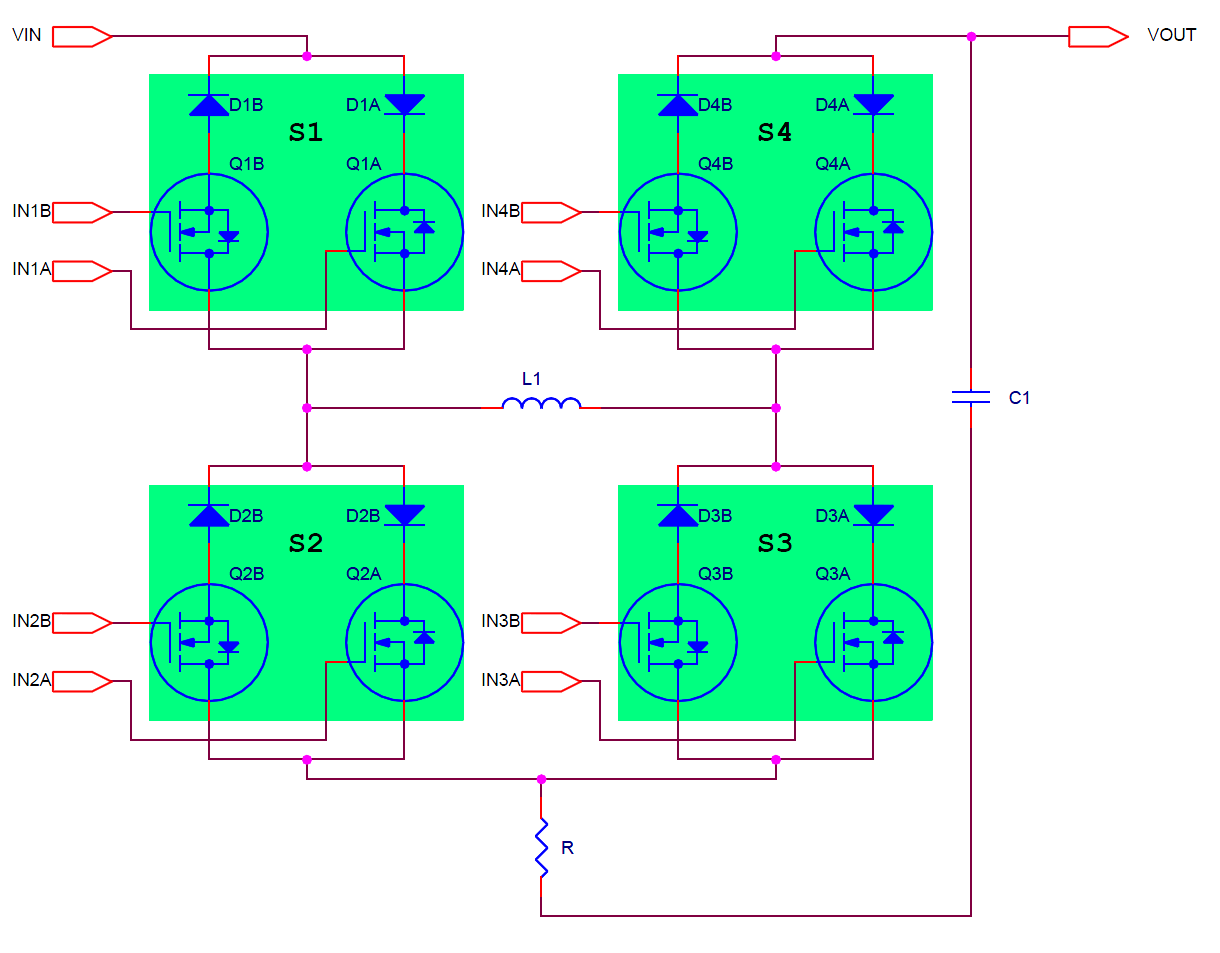
**3. Bridge Topology**

The principal topology of the converter is shown in Fig. 2. Each of the four switches, S1–S4, is bidirectional and consists of a pair of ultra-fast metal–oxide–semiconductor field-effect transistors (MOSFETs). A circuit in such a configuration can work independently in buck or boost mode. When the switch control signal is high, the transistors conduct and permit current to flow; when the switch control signal is low, the transistors are in the cutoff position. As depicted, bidirectional switches S1 and S2 operate as buck converters (step-down) using VIN as an energy source. Likewise, bidirectional switches S3 and S4 operate as boost converters (step-up). The switches active in each of these modes are summarized in Table I. When there are constraints, switch S4 acts in reverse to the S3 switch, and switch S2 is the reverse of S1. Because buck and boost converters use an inductor as an energy storage element, they have a period based on two sections: Ton – the inductor charge time, the time when the inductor current is rising and taking energy from the input; Toff – the inductor discharge time, the time when the inductor current is reduced while transferring energy to the output. The timing algorithm must also consider loads with cos(Φ)≠1; in other words, inductive and capacitive loads. Therefore, in our system, we need to consider not only the polarity of the voltage but also the polarity of the current. Because a phase difference between the voltage and the current is possible, there are four feasible states in each cycle; we refer to these as the four quadrants of the cycle. The polarities of the voltage and current in each of these quadrants is summarized in Table II.









**Fig. 2.**

The basic converter topology consists of four bidirectional switches.

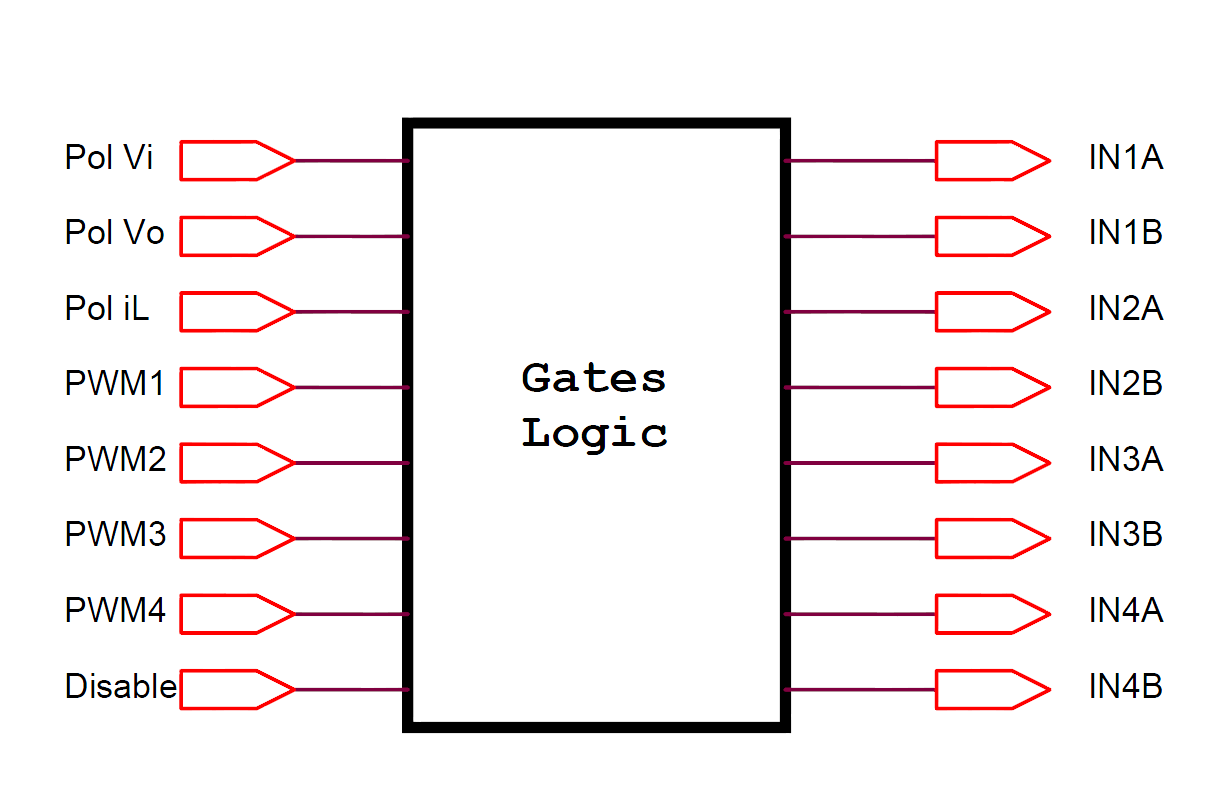
**TABLE I** The active and passive switches in each mode of the converter.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Mode | S1 | S2 | S3 | S4 |
| Buck | PH | PL | Off | On |
| Boost | On | Off | PH | PL |

**TABLE II** The four quadrants of the cycle.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Buck Polarity | | Boost Polarity | |
| Quadrant | VIN | IL | VOUT | IL |
| Q1 | **+** | **+** | **+** | **+** |
| Q2 | **+** | **-** | **+** | **-** |
| Q3 | **-** | **-** | **-** | **-** |
| Q4 | **-** | **+** | **-** | **+** |

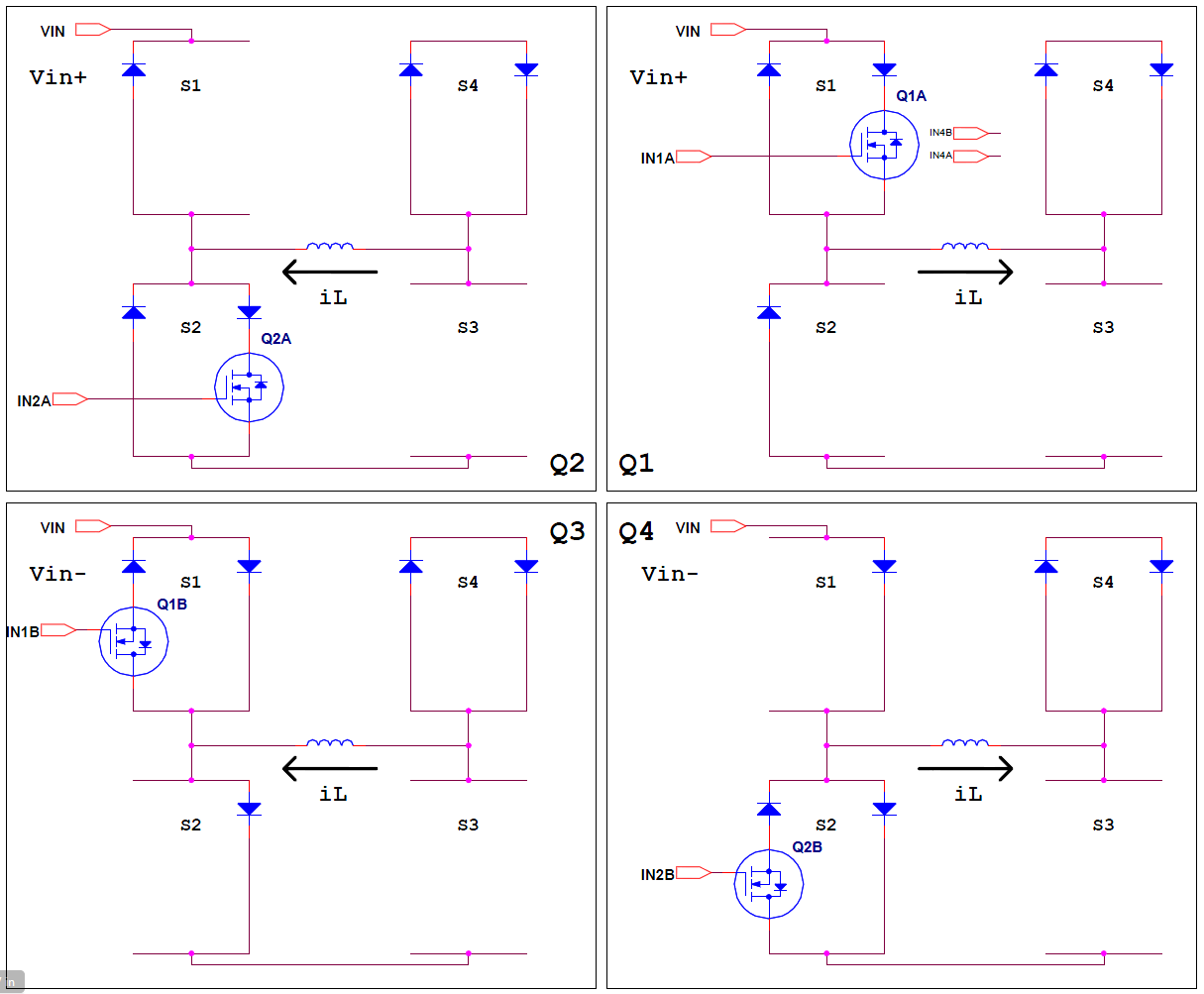
At any given moment, we need to determine the state of switches S1–S4 according to Table I. We then determine the polarity of each of the switches according to Table II. The polarity of a switch determines whether a transistor QA or QB will be active. In order to implement the control described above and combine the two tables, we need a high-speed digital circuit, which receives as its input the polarities of the voltages and current, and the pulse-width modulated (PWM) signals, and outputs the signals to the eight transistor gates (INnA, INnB) represented in Fig. 3, which schematically depicts the control logic block.



**Fig. 3.**

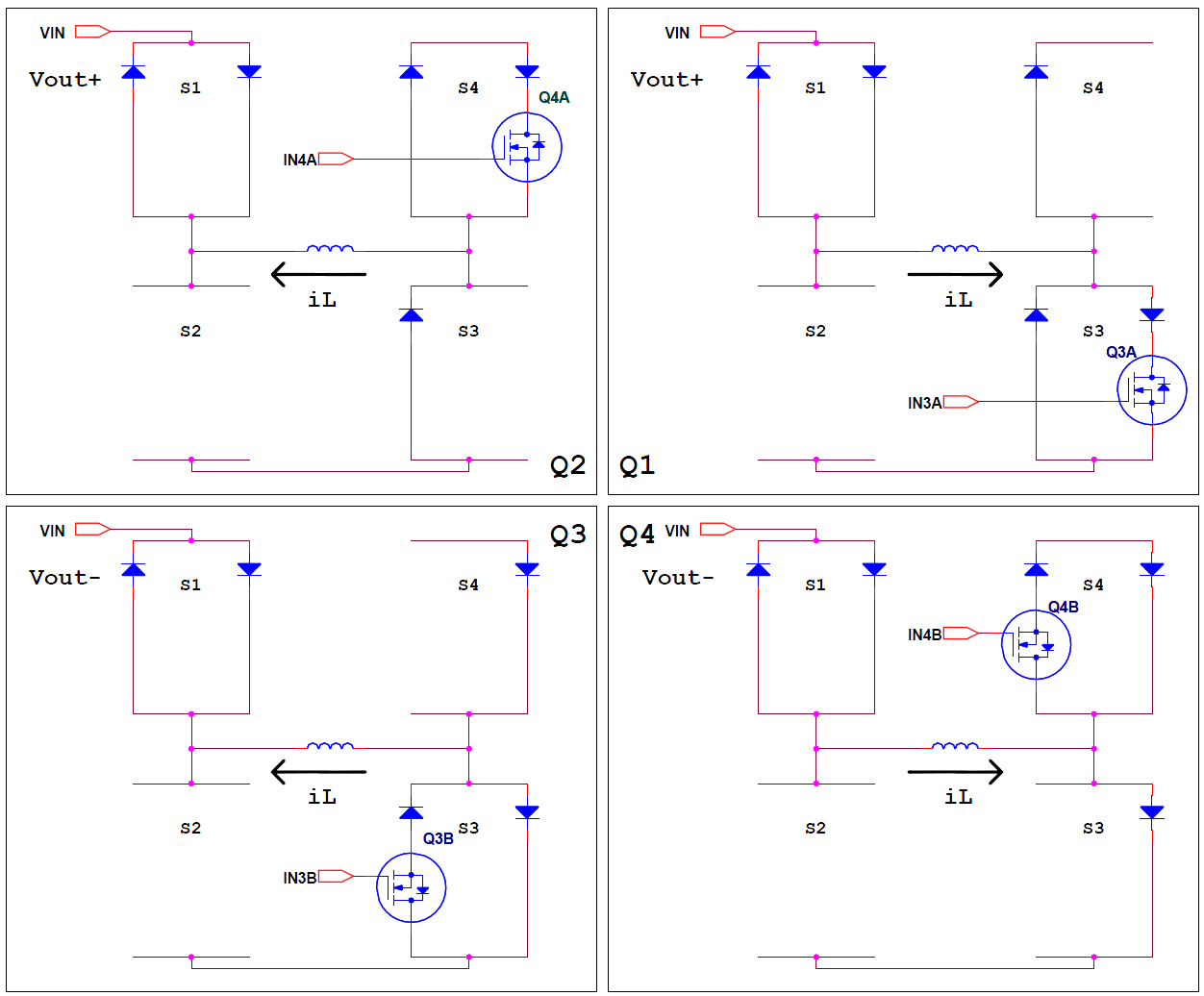
The gate logic block.

The polarity of the voltage detectors will be ‘1’ when the sensed voltage is above zero, and ‘0’ when the sensed voltage is below zero. The polarity of the current detector will be ‘1’ when the inductor current is flowing from input to output. Input switches S1 and S2 are activated according to input voltage polarity, while S3 and S4 are activated according to output voltage polarity. Fig. 4 depicts the configuration of the bidirectional bridge for the four quadrants depending on the input voltage, while Fig. 5 depicts the bridge configuration for the four quadrants depending on the output voltage. Only pulsed transistors are shown; a transistor that is always “on” or “off” is not shown in the figures: its series diode is either shown as connected or disconnected.



**Fig. 4.**

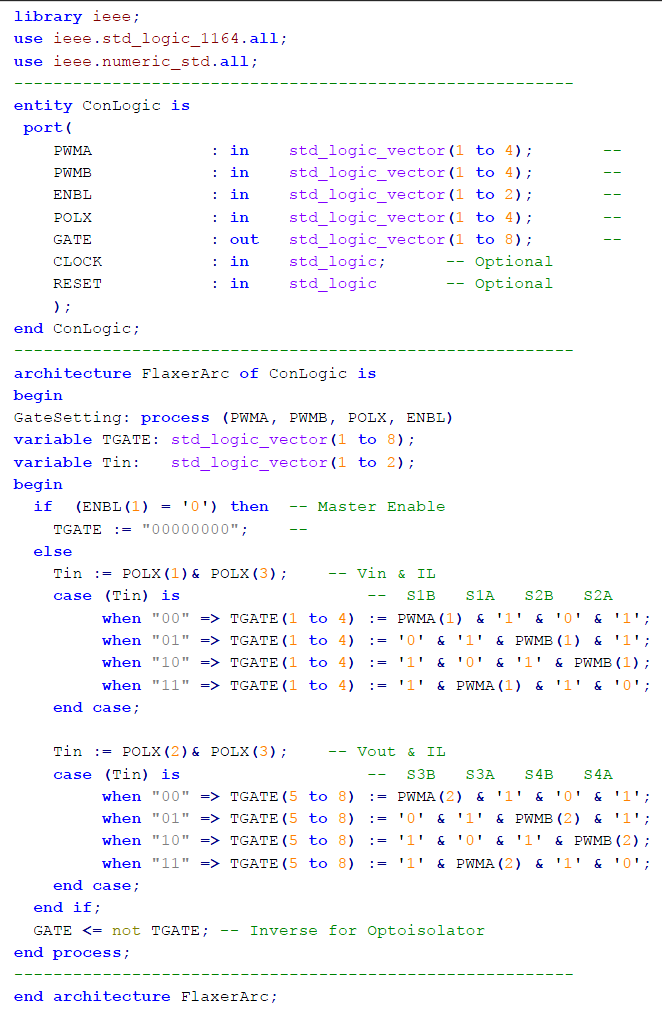
Buck configuration of the bidirectional bridge for the four quadrants depending on the input voltage. Transistors that are always “on” or “off” are not shown. In the positive half-cycle of VIN, the bridge passes between quadrants Q1 and Q2; in its negative half-cycle, the bridge passes between quadrants Q3 and Q4.



**Fig. 5.**

Boost configuration of the bidirectional bridge for the four quadrants depending on the output voltage. Transistors that are always “on” or “off” are not shown. In the positive half-cycle of VOUT, the bridge passes between quadrants Q1 and Q2; in its negative half-cycle, the bridge passes between quadrants Q3 and Q4.

To implement the digital logic block described in Fig. 3, 4 and 5, we used Lattice Semiconductor’s LCMXO256C complex programmable logic device (CPLD) [21], part of its MachXO family. This MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low-capacity field-programmable gate arrays (FPGAs): glue logic, bus bridging, bus interfacing, power-up control, control logic, and a response time of around 1 ns. These devices combine the leading features of CPLD and FPGA devices on a single chip. Lattice Diamond software and VHSIC Hardware Description Language (VHDL) were used to write the CPLD code for simulation and synthesis. Fig. 6 shows the VHDL code that implements the logic control circuit. Using a CPLD and VHDL code allows for flexibility in the hardware; the circuit can be extended and the functionality of the control circuit changed by software alone, without modifying the hardware.



**Fig. 6.**

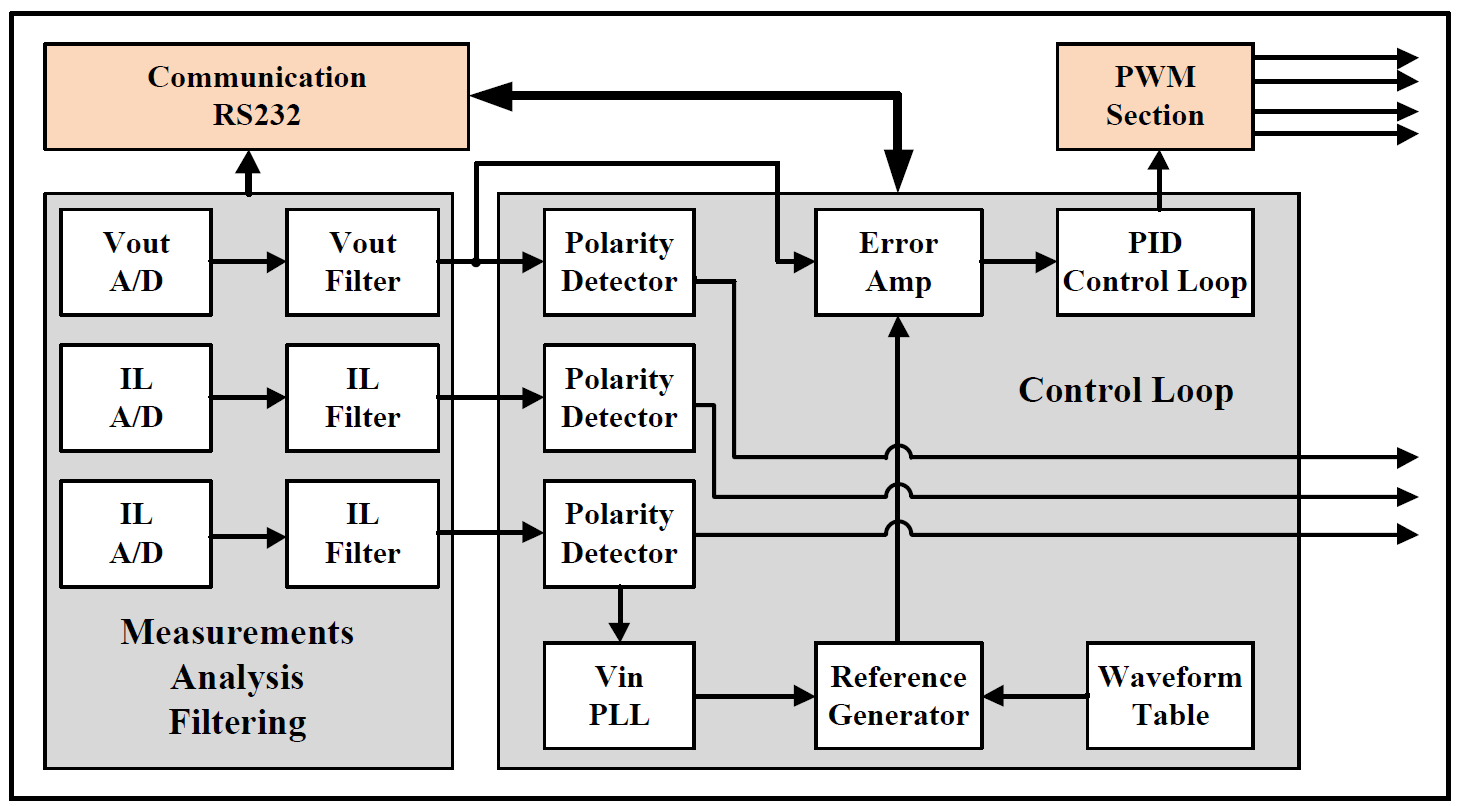
VHDL code to implement the control logic.

**4. DSP and Embedded Software**

For strategic reasons, we have chosen to implement the entire system via real-time embedded software running on a DSP. The embedded software includes the sampling mechanism, the digital filters, the PID control loop, the PWM timing mechanisms, the polarity detector, and communication functions. Fig. 7 shows the block diagram of the embedded software. In order to accomplish all of the described tasks in real time, we need a suitable high-speed processor with sufficient memory. In addition, the processor should contain high-resolution PWM units, a 32-bit timer, and fast analog-to-digital converter (ADC) units. The most suitable processor for our purpose is the Texas Instruments Delfino microcontroller [22]. This currently has several versions, running on clock rates of 150 to 300 MHz. Furthermore, versions are available with multiple cores. In our initial design, we used the TMS320F28335 150 MHz version (for the later design, the TMS320F28377D was preferred). This controller includes a floating-point unit (FPU), essential for real-time calculations of all our tasks, 512 kB of flash memory for programming, and 68 kB of SRAM for the data. It has 16 fast ADC channels with a conversion time of 80 ns, six enhanced capture (ECAP) units that can serve as 32-bit counters, peripheral interrupt expansion (PIE) that supports all peripheral interrupts, and a wide range of communication units (SCI, SPI, CAN, I2C). In particular, this controller includes several channels of enhanced high-resolution pulse-width modulation (HRPWM), with a resolution of 130 ps. The HRPWM unit has a trip-zone (TZ) mechanism to give continual protection in relation to the current and short circuits in the load. In addition to this TZ submodule, the microcontroller has a dead-band (DB) mechanism designed to drive switches in the full-bridge architecture. We used two complementary HRPWM channels of the DSP (PWM1, PWM2) to trigger the gate driver.

**4.1 Polarity Detector**

As represented in Fig. 7, the software is based on several interrupts in a well-defined hierarchy. The software’s highest priority interrupt is triggered by the PWM mechanism at the bridge's switching rate, which is 150 kHz. The PWM mechanism schedules the ADC unit that generates the interrupt at the end of the conversion. That is, in each PWM cycle, occurring every 6.7 μs, the 16 ADC channels are sampled. Three of these 16 channels involve sampling of the input voltage (VIN), the output voltage (VOUT), and the inductor current (IL). The rest of the ADC channels sample the input (IIN) and output (ISEN) currents, and several control values in the system for debugging. The samples of the first three channels (VIN, VOUT, and IL) are filtered by median and finite impulse response (FIR) digital filters. The filtered samples are then transferred to polarity detectors that are based on zero-crossing detection. In order to achieve accurate, reliable, and error-free polarity detection, the polarity detector contains a hysteresis mechanism and a blanking mechanism. The polarity detectors produce a logic ‘1’ in the positive half-cycle and a ‘0’ in the negative half-cycle of each signal. The logic signals are transmitted to the control logic unit.



**Fig. 7.**

Block diagram of the embedded software.

**4.2 Reference Generator**

The reference generator produces a unity-amplitude sinusoidal waveform (or any other selected waveform) with a frequency locked on the input signal (VIN). In order to save on real-time calculation, we calculated the sine values in advance and saved them in a lookup table in memory. This table contains 256 values (int16 type) for the complete sine cycle. Because we want 16-bit rather than 8-bit resolution, we performed a real-time linear interpolation between adjacent points in the table.

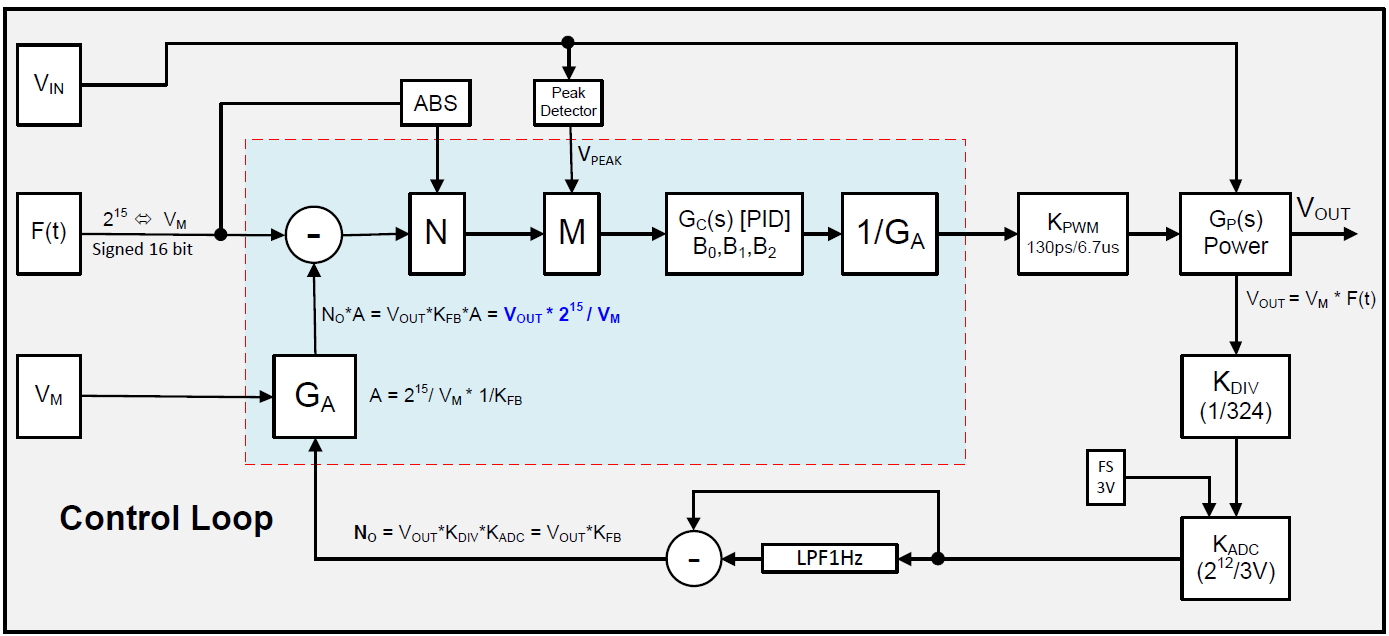
For software implementation of the PLL, we use two ECAP units that contain a 32-bit counter, counting at a rate of 150 MHz. One unit (ECAP5) is used as a general-purpose free-running clock in a system with a resolution of 6.7 ns, while the second (ECAP1) is used to lock in the input frequency. In addition to polarity, the VIN polarity detector calculates the period (frequency) of the input signal and its phase relative to the output voltage and current. Furthermore, the detector captures the timestamp of the zero-crossing event (from ECAP5).

Using the DSP’s TIMER0 unit, we generate two additional lower-priority interrupts, every 25 μs (Int25) and 200 μs (Int200). In the Int200 interrupt service routine (ISR), we perform closed-loop control of the ECAP1 period value to lock on the input voltage period time. This process gives us a result in which the value of ECAP1 represents the relative time of the input voltage cycle. Using this value, we obtain the pure mathematical sine value of the synthesized waveform from the lookup table.

**4.3 Closed-Loop Control – PID**

The most significant procedure in the program is the closed-loop control of the output voltage. Remember that our switching rate is 150 kHz, while the input's voltage frequency is 50 to 60 Hz. That is, the control frequency is 2500 to 3000 times greater than the controlled signal frequency. We have used dynamic loop gain to compensate for the alternating nature of the signal, so we can treat the input signal as constant (DC voltage) in the switching frequency time interval. Therefore, for any short time interval, we can treat the converter as a DC-to-DC converter, considering all the possibilities mentioned earlier. Therefore, the output voltage will be equal to the input voltage multiplied by the duty cycle for each short interval. In our system, the duty cycle is defined virtually as a real number (*R*) between 0 and 150 percent (0.0–1.5). Because the input and output voltages are continuously measured at a high rate, the DSP can determine in real time the working mode in which the converter is operating: buck or boost, so that the output voltage maintains the expression VOUT = *R* \* VIN over the entire range of values of *R*. Fig. 8 depicts the block diagram of the control loop, which includes the transfer functions of all the elements in the loop. The control function obtains the instantaneous value of the synthesized waveform F(t), the desired amplitude of the output voltage VM, and the detected peak of the input voltage VPEAK. The peak value, and the RMS values of the voltages and currents, are calculated continuously in the Int200 ISR.

We can, in this situation, work in an open loop and set the duty cycle to a constant value. In this case, the controller will operate as an unregulated electronic transformer: the output voltage will be a constant product of the input voltage. When working in a closed loop, one should take into account all the factors that are within the loop: the gain, the phase, and so on. In Fig. 8, we can see all of these factors: KADC is the gain of the ADC with a reference voltage of 3 V and resolution of 12 bits; KDIV is the attenuation of VIN buffer 1/324; KPWM is the gain of our PWM unit working in high-resolution mode at a rate of 150 kHz and a resolution of 130 ps. The GA block is the relative scale between the synthesized waveform and VOUT. The control’s transfer function, GC, is a two-pole two-zero (2P2Z) filter reduced to PID control using three coefficients, B0, B1, and B2. These coefficients are system-specific and not general, so their values need to be optimized.



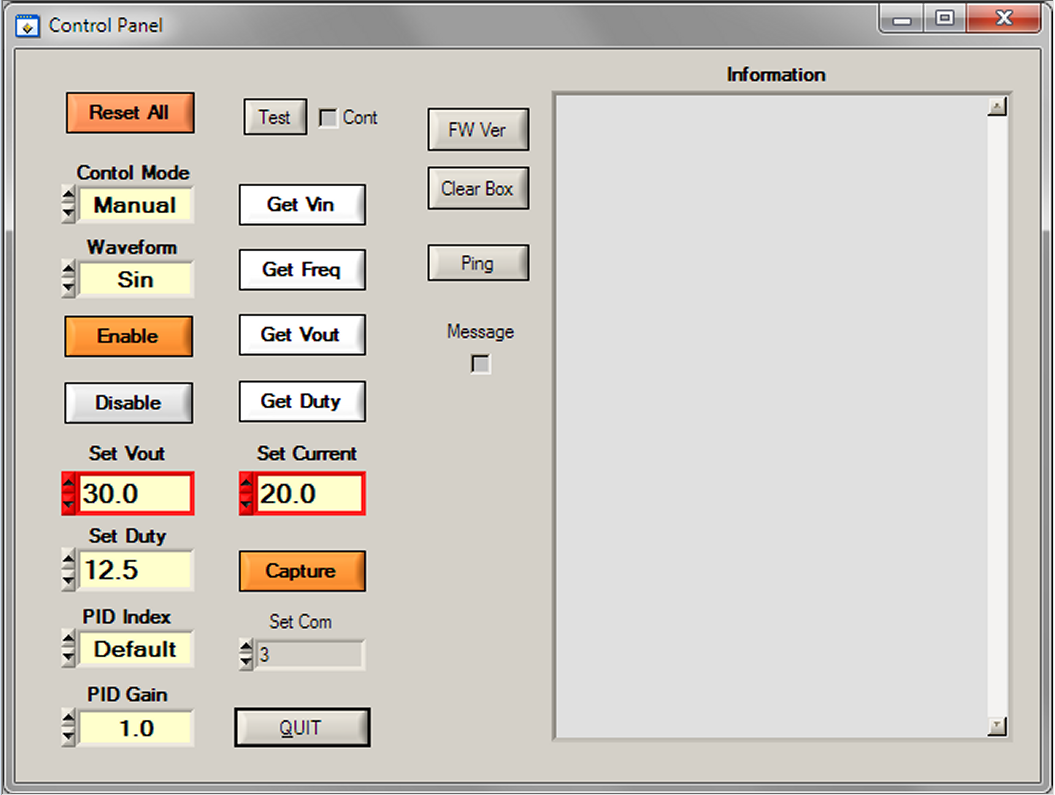
**Fig. 8.**

Block diagram of the closed-loop control.

For VOUT with a given amplitude VM, changes in VIN’s amplitude (VPEAK) change the loop’s overall gain. Because we want to keep the loop stable under all conditions, the control process normalizes the overall loop gain using VPEAK to eliminate its influence on the loop response (M unit). In the same way, we have the option to normalize the overall loop gain using F(t) to eliminate its influence on the loop response (N unit). The control loop runs in the Int25 ISR.

**5. Communication Software and User Interface**

To communicate with the converter, a control application was written using the C programming language and the National Instruments LabWindows/CVI software development environment [23]. The program, running on a PC, connects to the microcontroller via an RS-232 port. As depicted in Fig. 9, the GUI of the control software allows determination of the desired output voltage (Set Vout), the current limits (Set Current), the control mode (Closed Loop or Manual Open Loop), the waveform type (Sine or Triangular), the duty cycle for open-loop mode (Set Duty), and the PID coefficients (PID Index). It can also turn the controller on or off (Disable, Enable). In addition, the application can read the following parameters: input voltage (Get Vin), frequency (Get Freq), output voltage (Get Vout), and duty cycle (Get Duty).

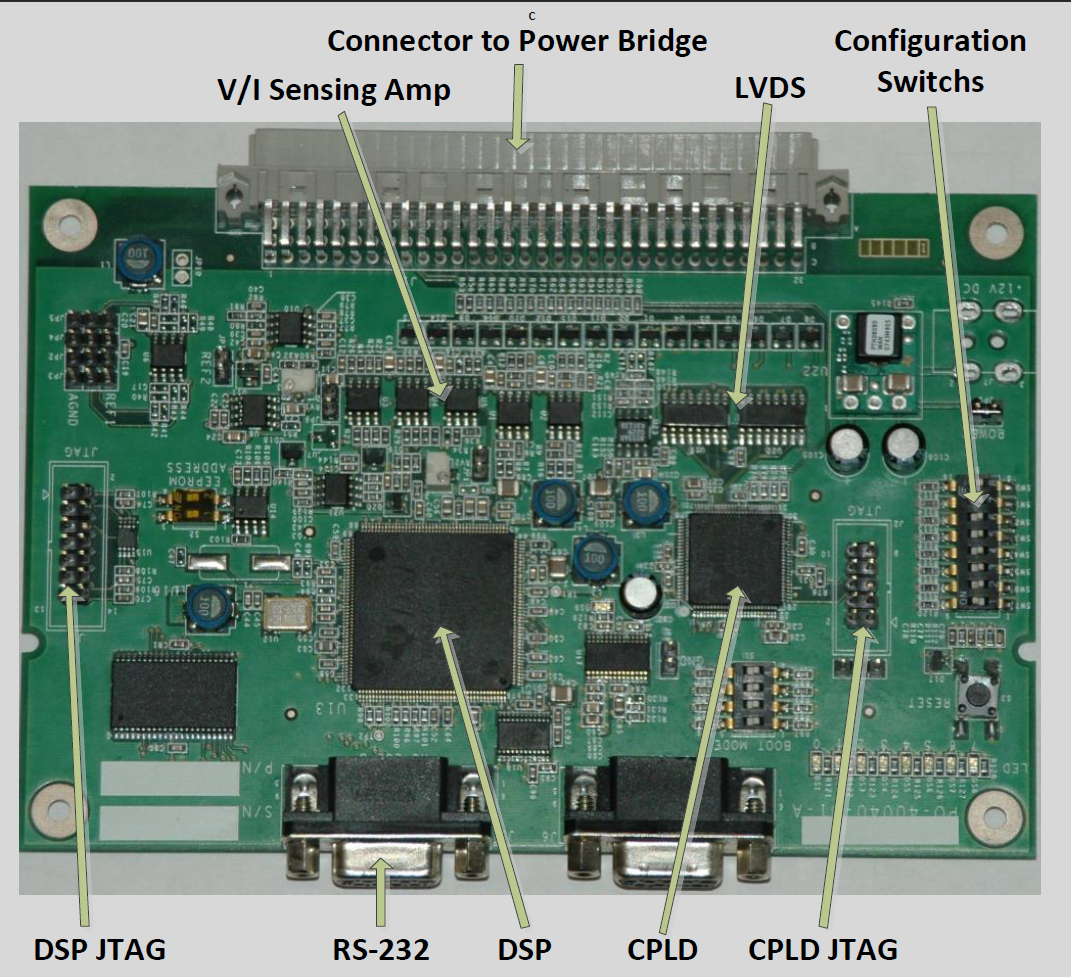


**Fig. 9.**

The software control panel is used to set and get the parameters of the converter.

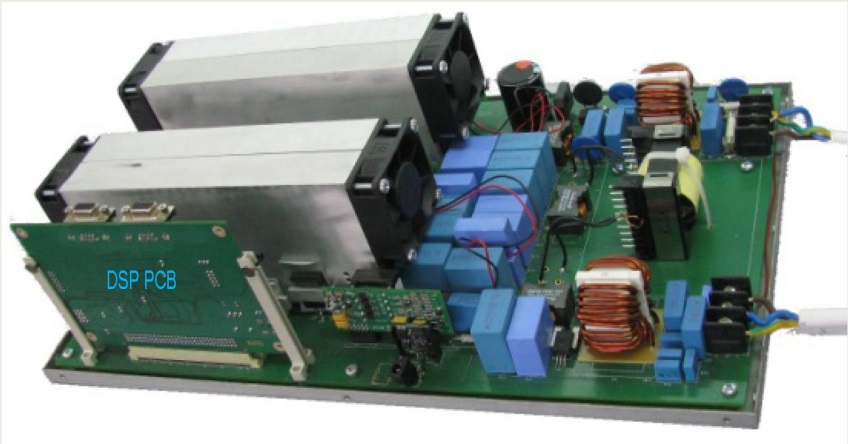
**6. Electrical Circuit**

In order to maintain flexibility, we split the electrical circuit into two partial builds on two separate printed circuit boards (PCBs). One PCB includes the digital control, consisting of the CPU and CPLD, and the other includes the bridge power devices, capacitors, inductors, auxiliary power supply, and other devices. Fig. 10 shows the PCB of the digital control unit with all of its components, and Fig. 11 shows the power PCB.



**Fig. 10.**

The PCB of the control unit with all of its components; the connector at the top connects to the analog power PCB.



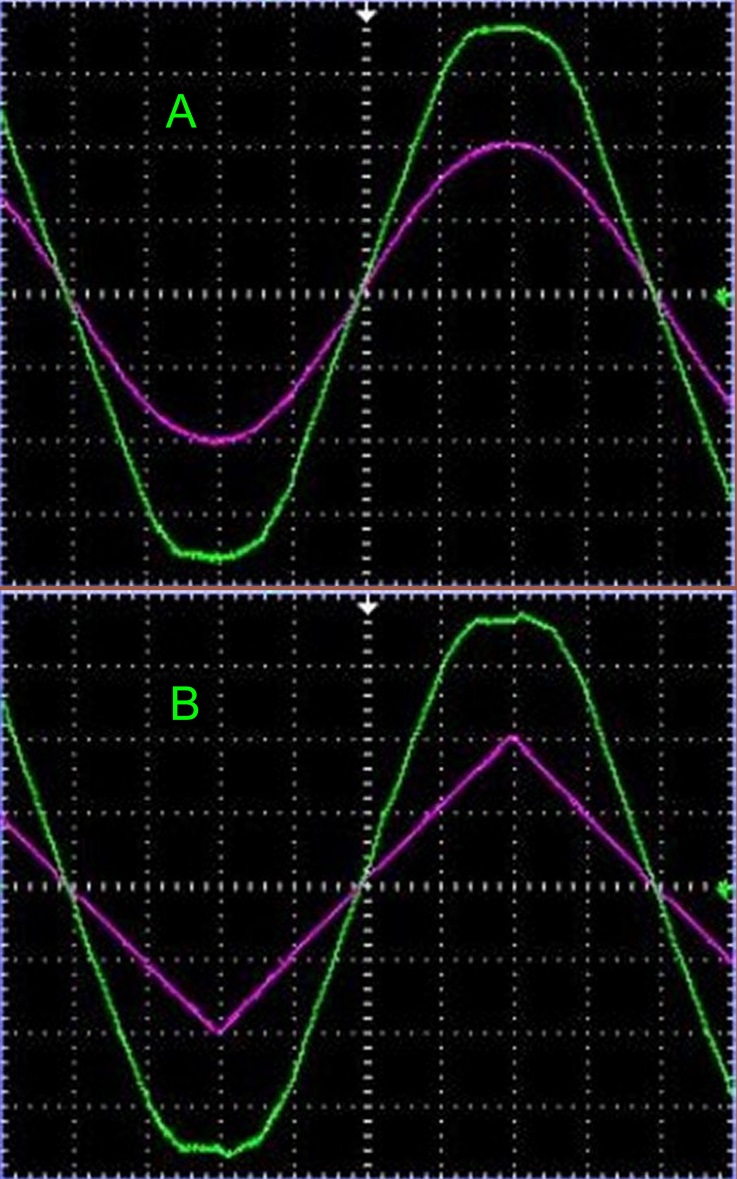
**Fig. 11.**

The power PCB includes the bridge, capacitors, inductors, and auxiliary power supply. On the lower left side, we can see the DSP-based control PCB installed on the connector. The dimensions of the power PCB are 25 x 40 cm, and its weight is 2.5 kg.

**7. Results**

The various system functions were tested to verify the performance and responsiveness of the electronics, and then to evaluate the system’s performance as a regulated electronic transformer. To adjust the input voltage, we used a Staco 3PN1520B Variac variable transformer [24]. Initial tests were conducted to check the operation of each part of the converter and then calibrate its PID coefficients. We used the control software to set the control mode to closed loop, the waveform to sinusoidal, and the peak output voltage to 100 V, while the peak input voltage was around 180 V, and the load was a resistor of 20 Ω.

After identifying the optimal PID coefficients, we measured the output voltage versus the input voltage, as shown in Fig. 12A. It can be seen that the input voltage is entirely unclean and contains distortions throughout the period. On the other hand, the output voltage shows a clean sinusoidal wave without distortion, locked to the input signal, at a peak voltage of 100 V as required. To illustrate the performance of the converter more dramatically, we repeated the experiment when the desired waveform was triangular, as illustrated in Fig. 12B. It can be seen that the input voltage is unclean, while the output voltage shows a clean triangular wave, locked to the input signal, with a peak voltage of 100 V.

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**Fig. 12.**

Traces of output voltage versus input voltage for closed-loop mode, a peak input voltage of 180 V, and a peak output voltage of 100 V: (A) sinusoidal waveform; (B) triangular waveform.

**8. Conclusions**

This work presents an innovative development of direct, stabilized, controlled, and protected AC–AC conversion. We have developed the first electronic transformer based on single-stage AC–AC conversion. The transformer we developed can lock onto any voltage (110 V or 220 V) with a frequency of between 45 and 65 Hz. The system we show is a single-phase one with a power of 4 kW in which the efficiency is greater than 97%.

**Acknowledgments**

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