In-House Accelerated Alpha Particles SER Testing and Failure Rate Calculation

White Paper

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Revision History

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| --- | --- | --- | --- |
| Version | Author | Date | Description of change |
| 0.1 | Deny Hanan | 24/03/2020 | Initial writing |
| 0.2 | Deny Hanan | 13/04/2020 | Update Practical Aspects  section |
| 1.0 |  |  | Formal release |
| 1.x |  |  | Minor updates |
| 2.0 |  |  | Major updates |
|  |  |  |  |
|  |  |  |  |

# Introduction

One of the reliability concerns in modern electronics is related to single-event upsets (SEU) and soft errors (SER). These problems are due to the flipping of digital bits in memories and/or in sequential logic. [1]

This reliability phenomenon occurs as a result of an interaction between high energy radiation particles and the IC's active area.

This white paper describes the nature of alpha particle radiation and its source in semiconductors, and it presents a new quantitative methodology of in-house accelerated SER testing based on the registered patent number 10578669 [2].

# What Alpha Particles are

Alpha particles are a type of radiation that is generally produced by radioactive decay of naturally occurring radioactive impurities. These impurities are present in trace amounts in materials that are used for manufacturing microelectronics, for its packaging, and for the assembly of electronics.

Alpha particles, also called alpha rays or alpha radiation, consist of two protons and two neutrons bound together into a nucleus, identical to the helium nuclei. The symbol for the alpha particle is α or α2+.

Because alpha particles are identical to helium nuclei, they are also sometimes written as *He2+*  
or  indicating a helium ion missing its two electrons with a +2eV charge. If the [ion](https://en.wikipedia.org/wiki/Ion) gains two electrons from its environment, it becomes a neutral helium atom, . This same physics holds for alpha particles; if an alpha particle gains two electrons from its environment, it becomes a neutral helium atom . [3]

# Alpha Particle Source

Advanced packaging technologies such as Flip Chip (FC), 3D Chip on Chip (CoC), Package on Package (PoP), Through-Silicon Via (TSV), and Chip Size Package (CSP) are commonly used, resulting in a close interaction between the IC and its packaging materials. [4]

|  |  |
| --- | --- |
| **Material** | **Range [µm]** |
| Air | 39,900 (3.9 cm) |
| Si | 29 |
| Polyimide[5] | 28 |
| Resist [5] | 24 |
| Al | 24 |
| Pb | 16 |
| Cu | 12 |
| Si2O | 12 |
| Au | 9 |
|  |  |
| Table 1. Range of alphas in some materials | |

The IC and packaging materials contain trace amounts of radioactive impurities that emit alpha particles during decay. The emitted alpha particles are emergencies and can travel through semiconductor materials to the range of tens of micrometers.

Table 1 presents some examples of the penetration range of typical 5.4MeV alpha particles; they can penetrate ~29µm in the Si layer or easily pass through thin metal films.

Alpha particle emission is *an intrinsic phenomenon* related to construction material impurities. Even the ultra-high-purity materials, which are used in semiconductor manufacturing, contain a small portion of impurities that emit alpha particles and may cause soft errors.

The primary source of alpha particles is packaging material, such as mold compounds, underfill, solders, and in some cases also semiconductor fabricating materials. The industry is facing contradictory technology trends; on one hand, material manufacturers have created low-alpha materials; on the other hand, the semiconductor technologies are scaling down and the power-supply is dropping. The sensitivity to alpha particles that causes soft errors for typical microelectronics using ultra-high-purity materials is estimated to be in the range of 100-1,000 failures per 109 device hours per cm2 (FIT/cm2) [1] .

For reference, see Table 2for some typical informative alpha emission rates for various materials that are used in the semiconductor industry. The center column of Table 2presents information from a worldwide semiconductor manufacturer, and the right column presents references from an important standard.

|  |  |  |
| --- | --- | --- |
| **Material** | **Emissivity (#/cm2/hr)** [1] | **Emissivity (#/cm2/hr)** [6] |
| Fully processed wafers | < 0.001 | < 0.0004 |
| 20-μm-thick AlCu metal | < 0.001 | < 0.0003 |
| 30-μm-thick Cu metal (UBM) | < 0.002 | < 0.0003 |
| Flip-chip underfill | <0.002 - <0.001 | <0.004 - <0.0005 |
| Packaging mold compound | < 0.024 - <0.001 | < 0.024 - <0.0005 |
| Lead (Pb) based solders | <7.200 - <0.002 | <7.200 - <0.0009 |
| Lead-free solders |  |  |
|  |  |  |
| Table 2. Typical alpha-emission rates from various materials | | |

## Package Materials

Packaging materials, such as molding compounds, underfills, and metal distribution layers, are contributors to soft errors, but the soldering materials are the main contributor.

Low alpha soldering, such as lead-free solders, originally started as an environmental issue and rapidly became an alternative for surface mount assembly applications. The lead-free material, that by nature does not emit alphas, demonstrates some reliability weaknesses relative to lead technology, such as fatigue, resistance to temperature-cycling, and robustness to extreme temperatures.

For that reason, some exceptions still use material containing a significant enough percentage of lead to result in alpha emission; for example, the bumps for wafer-level arrays and flip-chips contain significant amounts of lead for mitigating the reliability problems that alternative materials have demonstrated. The content of lead in advanced packaging technologies results in significant alpha emissions in a close distance to IC active areas. [5, 4]

This continuous dependence on the use of lead-containing solders for wafer level and flip-chip packaging, the importance of use of underfill for these applications, the scaling down of semiconductors and subsequent power drop are indicators that the challenge of SER due to alpha emission remains present regardless of the ''lead-free" trend of the industry.

## Wafer level

An interesting source of alpha particles in semiconductors is the secondary radiation induced from the interaction of low-energy cosmic-ray neutrons (thermal neutrons) with unstable isotopes of boron (10B).

Boron is used as a P-type diffusion and implant species in silicon in the formation of boron-doped phosphosilicate glass (BPSG) dielectric layers and as a formation or carrier gas for several processes.

After absorbing the cosmic neutron, the 10B nucleus breaks apart with an accompanying release of energy in the form of an excited 7Li nucleus and an alpha particle. The alpha particle is emitted with energy of 1.47 MeV, as illustrated in Figure 1. The mobility range of the alpha is short (~1.6µm in Si2O and ~4µm in Si) but due to its proximity to the active areas, it may, in some cases, force a soft error.

Figure 1. Secondary radiation of boron

# Soft Errors (SER) Mechanism

Soft errors are the change in logic state of a digital transistor or memory cell due to the interaction of energetic particles with the IC. The SER (usually) does not harm the device; the changed logic state remains erroneous until refreshment of the data. Soft errors may affect dynamic data transfer like static data applications.

Semiconductor designers put significant effort into mitigating the SER phenomenon by implementing error detection and correction algorithms and by using ultra-high-purity materials. Understanding the exact soft error rates allows the implementation of the required mitigation techniques and avoidance of under/over engineering.

The SER due to alpha particles is generated by striping electrons from atoms, such as 28Si. The alpha particle moves around until it incorporates two electrons and converts into a neutral atom, which then gradually diffuses through the crystal lattice and escapes into the atmosphere. Due to the stopping mechanism, alphas produce charges along their path, leaving a trail of electrons and holes. The electron-hole generation takes place within 1µm of the alpha's track. When enough electrons are knocked out along the alpha’s path and accumulated in the IC, it flips digital bits in memory and/or in sequential logic, switching its state and resulting in a “soft error.” [6]

# SER Testing Methodology

SER is an intrinsic phenomenon due to the trace amounts of radioactive impurities present in semiconductors. This intrinsic SER phenomenon must be considered during design and characterized before mass production. SER testing is a one-time characterization for new devices and is reiterated after any major change of existing devices.

The foundational Joint Electron Device Engineering Council (JEDEC) issued the Stress-Test-Driven Qualification of Integrated Circuits [7] standard that provides guidelines for qualification of general purpose ICs. This specification indicates that an alpha particle characterization is required as part of new IC qualification. The JEDEC test method for the alpha source accelerated soft error state is described in JEDEC89-2A [7, 8]. These JEDEC specifications are actually the baseline for segment specifications in many different markets.

The MIL-STD-883 has instructions for packaging induced soft error testing in TM 1032 for military and space applications and the standard ISO 26262 for road vehicle automotive calls "to thoroughly analyze and make sure to address possible safety related transient failures." [9]

These specifications are key representatives among many others in existence. The main aim of all SER testing specifications is to extrapolate experimental data to use conditions and to classify the soft error failure rate due to the intrinsic existence of alpha particles in the given device.

Because alpha emission during in-use conditions is low, the extrapolation of the failure rate at the in-use condition may last a long time. Alternatively, accelerated testing provides the required information in a reasonable time. It is done by exposing the Device Under Test (DUT) to a significant alpha particle flux, counting the number of errors due to this accelerated flux, and extrapolating the failure rate to actual operating conditions.

The following paragraph explains some of the engineering considerations of this methodology.

|  |  |
| --- | --- |
| *NOTE* | *Alpha particle SER data cannot be used to predict high- or low-energy neutron cosmic-ray-induced failure rates. Conversely, neither can high-energy neutron nor low-energy neutron SER data be used to predict alpha-induced failure rates.*  *An overall assessment of a device’s soft error sensitivity is complete only when the alpha* and *high- and low-energy neutron induced failure rates have been accounted for.* |

# Failure Rate Calculation

Typically, the SER is measured by the number of failures in 109 device hours (FIT). One FIT is a single failure in 109 operation hours, which is the same as one failure in 109 devices after one operation hour.

Good engineering practice is to normalize the FIT results to different densities, for example, FIT/Mb or FIT/bit for static measurement or FIT/Mb/sec for data flow.

## Failures in Time (FIT) Calculation

Failure In Time (FIT) is a standard industry model. It is calculated by dividing the total number of failures or rejects by the total accelerated device time of operation.

The total accelerated device hour is the number of tested units multiplied by the test time and acceleration factor.

## Acceleration Factor (AF)

Acceleration factor (AF) is defined as the ratio of the measured failure rate of the DUT at high alpha flux relative to the failure rates of identical devices at in-use condition, considering that the same failure mechanism is triggered.

A basic, alpha particle source AF is simply the ratio of the number of alpha particles per unit time emitted by the source and those emitted by the packaged IC [8]

The AF can vary in a large range; it can reach the level of 109 and even higher orders of magnitude. In practice, these large AFs mean the possibility to simulate tens of operation years at in-use condition within seconds of accelerated testing.

## Geometry Factor

Accelerated alpha soft error testing is done by placing a controlled alpha source on top of the DUT.

Due to the nature of the alpha particles and the geometry of the setup, the number of alphas that will reach the device is affected in many ways, such as self-absorption, backscattering, and electrical column interaction.

However, the following two aspects are the dominant parameters that affect the number of alphas that will reach the DUT.

The first is the medium between the source and the DUT. The medium, such as air, may scatter and absorb some particles. To minimize the effect of the medium, the fixture for testing is evacuated in order to minimize the interaction of alphas with the environment of the medium. The medium is usually air, but in some cases for specific engineering purposes, different environmental media may be considered.

The second aspect concerns the size and shape of the source relative to the DUT, and the distance between them determines what fraction of alphas will hit the DUT [10]. This is called the geometry factor and in some cases is a solid angle.

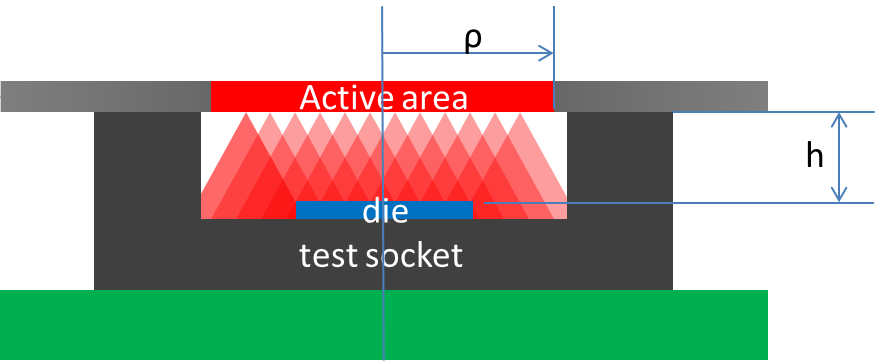


Figure 2: Setup cross section

The geometry factor for a disk shaped source and rectangular DUT is a general model (calculated for the specific set-up):

where *h* is the distance between the source and the DUT, and *ρ* is the radius of the source (see Figure 2).

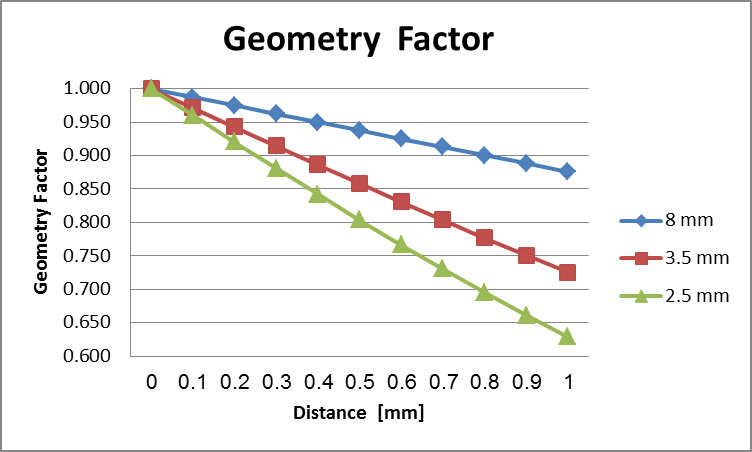


Figure 3: Geometry factor for radiuses of different sources

## Confidence Intervals

The confidence interval is a statistical interval around the sampled data point estimation that presents a band of results containing the true value. For example, a 95% confidence interval means that 95% of the calculated intervals from the sampled data contain the true (but actually unknown) value, while 5% do not contain the true value. A higher level of confidence results in a wider confidence interval.

In soft error testing, two models exist; the first tests for a predefined period of time, and the second tests for a predefined number of failures. The difference in testing mode also defines the calculation method of the confidence bounds.

For a predefined testing time, the lower one-tailed confidence interval is:

For a predefined number of failures, the lower one-tailed confidence interval is:

where *α* is the level of risk and is equal to 1-confidence; for confidence of 95%, *α* = 0.05; (note the different use of the term, alpha); and *r* is the number of failures.

Because the confidence interval calculation depends on the number of failures (r), the predefined test time mode assures the estimation of a confidence band even for no failure experiments, while the predefined number of failure experiments assures a more realistic confidence bound estimation.

# Practical Aspects

## Test Duration

Consider a test for a predefined period of time or a predefined number of errors. The predefined testing period provides information even if no failures are observed (via confidence bound calculation). The predefined number of failures testing mode may last for long trials, if no testing time limitations exist. The second testing mode is preferred. If test time is limited, then the first testing mode provides reasonable results.

## Acceleration Factor Estimation

For calculating the acceleration factor, information regarding the emission rates of all construction material is required, especially for main alpha emission contributors, including mold compounds, underfill, and soldering materials.

If the above information is unavailable, estimations of worst-case scenarios can be done according to the data in Table 2.

## Die Preparation

Two significant sources of alphas in semiconductors are the molding compound and the underfill material; on the other hand, these materials may also stop external alphas.

Due the above facts and for precise estimation of SER due to alphas, an exposed die without underfill is mandatory. A dedicated engineering package is preferred, but alternatively, decapsulation is an option.

## Dynamic vs. Static Testing

Dynamic test relates to sequential logic IC and static test relates memory related data, Modern systems in chip IC contain both IP types. List of IP and its standard use duty cycles is needed in order to design proper test patterns.

## Error Detection and Correction Internal Mechanisms

Many modern ICs contain error detection and correction mechanisms. For efficient SER testing, it is important during the test to have the option of disabling data correction and enabling error detection.

## Bias Voltage

The soft errors are usually sensitive to voltage operation. Consider an operation in the worst case scenario that usually involves minimum voltage operations.

## Data Refresh

To further detect errors and correct the refreshment of data commonly used in ICs, make sure to disable data refreshment before counting the number of errors and consider intermediate refreshment cycles during testing for enhancement.

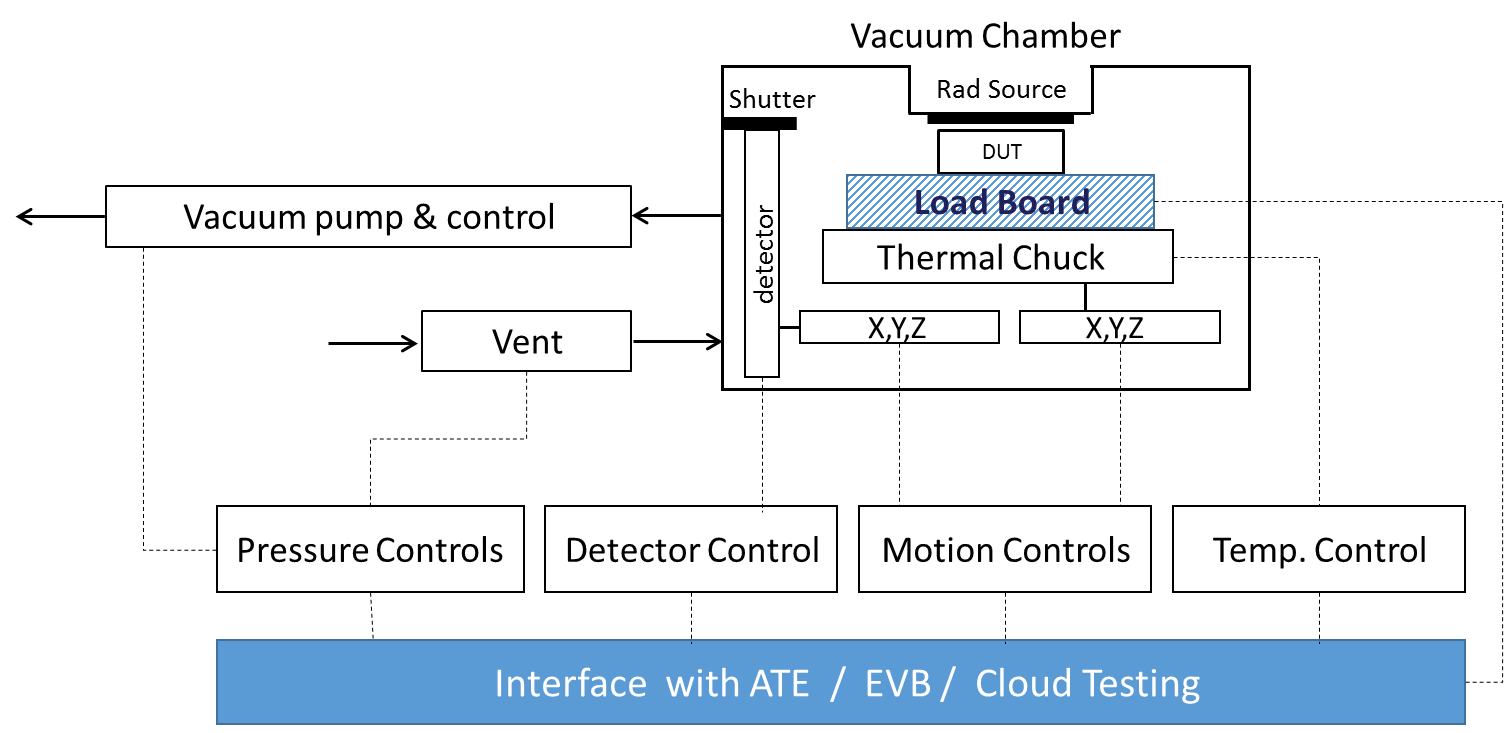
## DUT board hardware

Design the hardware to support the testing patterns, test temperature, junction temperature, and testing speed.

# Regulatory Limitations

Materials that emit alpha particles are controlled via the Ministry of Environmental Protection and the Ministry of Labor, Social Affairs and Social Services. Only certified personnel can handle these materials. Deny Hanan holds the required permissions.

# SER test fixture



1. Alignment of source with respect to DUT active area tested.
2. A description of any shadowing which might affect the final result by obstructing some of the source flux.
3. Source-to-die spacing.
4. Estimate of the alpha flux reaching the active device surface.

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