Principles Design and Implementation of Direct AC to AC Power Converter – Regulated Electronic Transformer

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**Abstract**

In the last three decades, following the development of technology, the reduction of dimensions, and the reduction of the costs of electronic components, switching power converters have taken the bulk of the energy conversion market. This market, in principle, includes four types of conversion: DC-DC, DC-AC, DC-AC, and AC-AC. While the first three are implemented directly in a single conversion. The fourth type is implemented in an AC-DC-AC dual conversion, requiring two AC-DC and DC-AC serial converters. This article will present an innovative development of direct, stabilized, controlled, and protected AC-AC conversion. We have developed the first electronic transformer based on single AC-AC conversion - this unique topology, which combines high efficiency along with the advantages of dual-conversion power quality protection. The transformer we developed can lock on any line voltage (110 V or 220 V) with a frequency between 45 and 65 Hz. The stabilization is done by fast PWM technology that is implemented by two-way fast solid state switches. The control is implemented by a 150 MHz digital signal processor (DSP). The transformer has full-automatic digital protection against overcurrent and short-circuits on the outputs. The system we built in the first stage is a single-phase with a power of 4 kilowatts where the efficiency is better than 97% and the weight and the volume are about one-tenth of an electromechanical transformer.

**Keywords**: AC-AC Converter; Electronic Transformer; Power Converting.

**1. Introduction**

Following the technology development - in reducing the dimensions and the costs of electronic components - switching power converters have taken the bulk of the energy conversion market. This market, in principle, includes four types of conversion: regulator (dc-dc), inverter (dc-ac), switching power supply (ac-dc), and an electronic transformer (ac-ac). While the first three are implemented directly in a single conversion. The fourth type is implemented in an ac-dc-ac dual conversion, requiring a rechargeable battery and two serial converters (ac-dc and dc-ac).

Worldwide damages caused due to voltage disturbances are estimated at billions of dollars. The worldwide economy is losing around 30 billion dollars a year to power quality phenomena. Worldwide phenomena of voltage fluctuations (sags, swells, surges, impulses, and harmonics) can result in considerable downtime, and enormous expenses as the customer manually reset the equipment and “cleans up” manufacturing processes disrupted.

Over the past two decades, work has been published on the subject of AC to AC converting [1]-[20]. The articles discussed single-phase conversion or multi-phase conversion, two-stage and single-stage conversion. None of them showed a real-time synthesis of alternating voltage from a pure reference waveform.

We were looking to replace traditional unreliable and expensive electro-mechanical conversion technologies with compact, reliable, and accurate switching technology while staying green and cost-effective. Our regulated electronic transformer (RET) is a single-stage ac-ac converter that will herald a new era in ac conversion. The RET is optimal for power quality conversion, energy mixing, and energy saving in industrial, commercial, and residential applications. It can replace the following transformers: autotransformers, buck-boost transformers, Ferro-resonant transformers, a replacement for all electro-mechanical regulators, a replacement for UPS’s where a backup is not needed. The RET converts ac inputs voltage while regulating ac output voltage with only a single converting stage between input and output. We developed and built a single phase 5 kW converter that shows regulation with converter efficiency of 98%, wide input voltage range of ±50%, and high power density to demonstrate the technology when the weight and the volume are about one-tenth of an electromechanical transformer.

**2. System Architecture**

The equivalent of our regulated electronic transformer building block is an autotransformer where output voltage could vary in the range of 50%-150% of input voltage when the response time is less than 100 us. At the same time, the size and the weight are significantly lower compared with standard switching converters. Appling, a high-speed close loop on such a switching transformer, enables synthesizing pure sinusoidal output waveform independently of the input voltage waveform. Figure 1 describes the high-level block diagram of our converter. The input voltage is fed into a filter and passes through a switching network, capable of step-up or step-down the voltage. The chopped voltage generated by the switches is then fed into an output filter to produce a clean output voltage. Additionally, the input voltage is fed into a phase lock loop (PLL) that is locked onto the input frequency and produces a pure mathematical reference of a sinusoidal (or another) waveform for the output voltage to be compared with.

A real-time digital signal processor (DSP) is used to close the loop on the output voltage to keep the output voltage proportional to the reference voltage. The result is a pure sinusoidal output waveform, without any disturbances and harmonics free. The output is maintained stable as long as the input voltage is within 50% to 150% of the desired output voltage, even if it is not a sinusoidal waveform; for example, it can be a square wave.

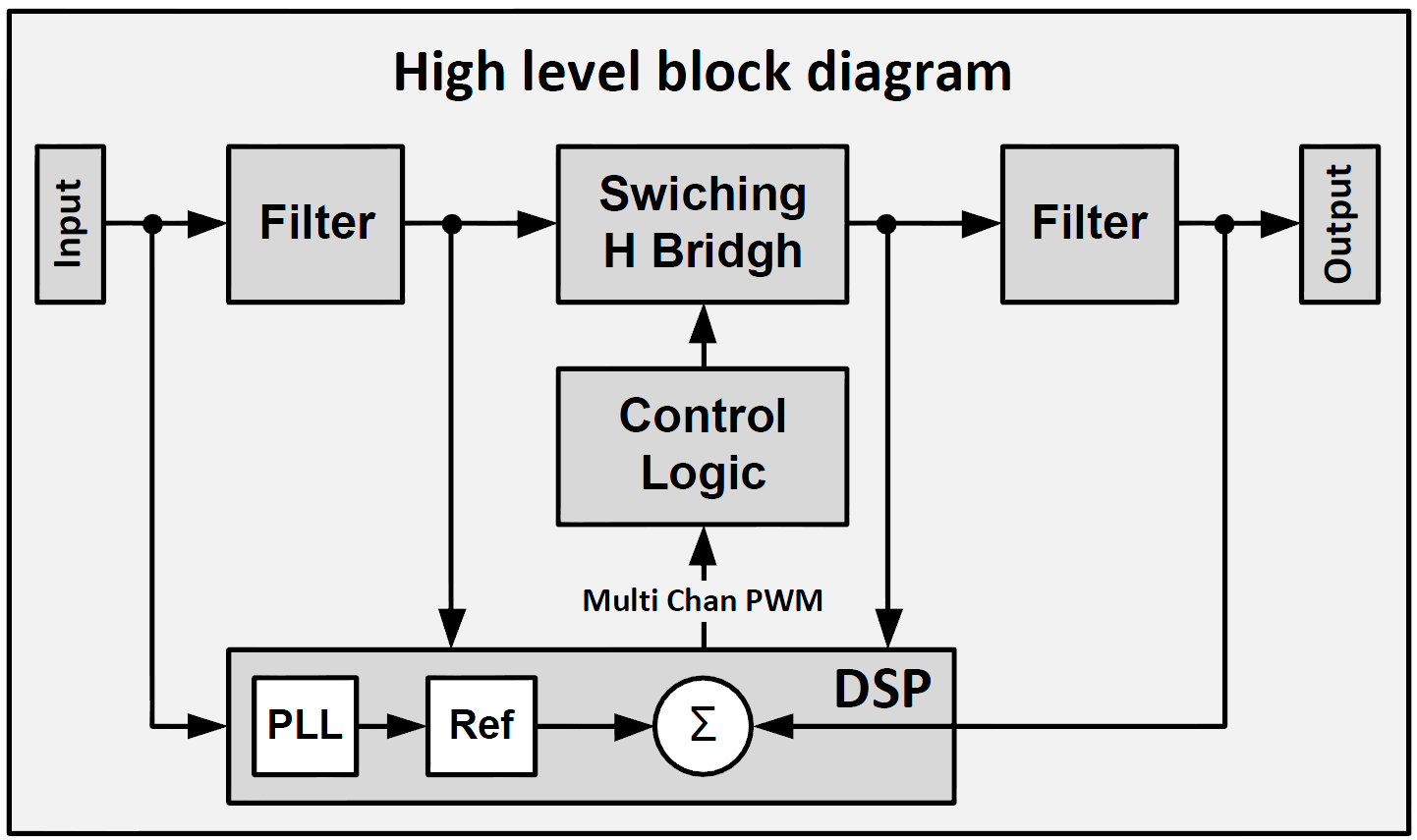


Figure 1 – High-level block diagram of the direct ac-ac converter.

**3. The Bridge Topology**

The principal topology of the converter is shown in Figure 2. Each of the four switches S1–S4 is bi-directional and made of an ultra-fast metal-oxide-semiconductor field-effect transistor (MOSFET). A circuit in such a configuration can independently work in buck or boost mode. Each of the bidirectional switches S1, S2, S3, and S4, comprises a pair of transistors. When the switch control signal is high, the transistors conduct and permit the current to flow. When the switch control signal is low, the transistors are in the cutoff position. As depicted, bidirectional switches S1 and S2 operate as buck converters (step-down) using Vin as an energy source. In the same way, bidirectional switches S3 and S4 operate as boost converters (step-up). The active switches in each mode described above are summarized in Table 1. When there are constraints, the S4 switch is opposite to the S3 switch, and the S2 switch is opposite to S1. Since buck and boost converters use an inductor as an energy storage element, they have a period that bases on two sections: Ton – the inductor charge time, the time when the inductor current is rising, and taking energy from the input; Toff – The inductor discharge time, the time when the inductor current is reduced while transferring energy to the output. The timing algorithm must also consider loads with cos(Φ)≠1, in other words, inductive and capacitive loads. Therefore, in our system, we need to consider not only the polarity of the voltage but also the polarity of the current. Since a phase difference is possible between the voltage and the current, there are four possible states in each cycle - we call them the four quadrants of the cycle. The polarity of the voltage and current in each of the quadrants is summarized in Table 2.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Mode | S1 | S2 | S3 | S4 |
| Buck | PH | PL | Off | On |
| Boost | On | Off | PH | PL |

TABLE 1: The active and passive switches in each mode of the converter.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Buck Pol | | Boost Pol | |
| Quarter | Vin | iL | Vout | iL |
| Q1 | **+** | **+** | **+** | **+** |
| Q2 | **+** | **-** | **+** | **-** |
| Q3 | **-** | **-** | **-** | **-** |
| Q4 | **-** | **+** | **-** | **+** |

TABLE 2: The four quadrants of the cycle.

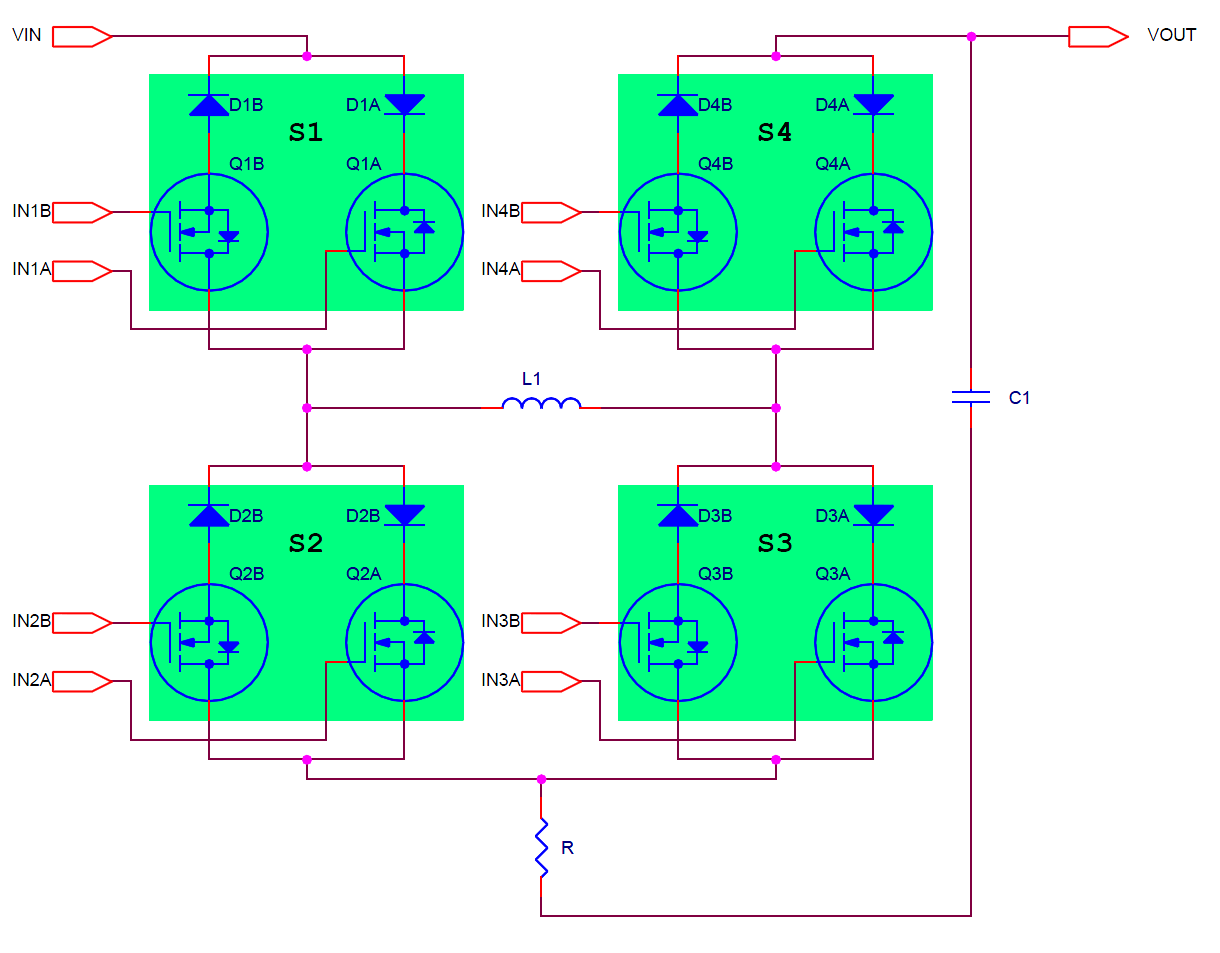


Figure 2 – The basic converter topology consists of 4 bidirectional switches.

At any given moment, we need to determine the state of the switches S1 - S4 according to Table 1. Then determine the polarity of each one of the switches according to Table 2. The polarity of a switch determines whether a transistor QA or QB will be active. In order to implement the control described above and combine the two tables, we need a high-speed digital circuit, which receives at its input the polarity of the voltage and current, and the PWM signals; and outputs the signals to the eight transistors gates (INnA, INnB) shown in figure 2. Figure 3 schematically depicts the control logic block.

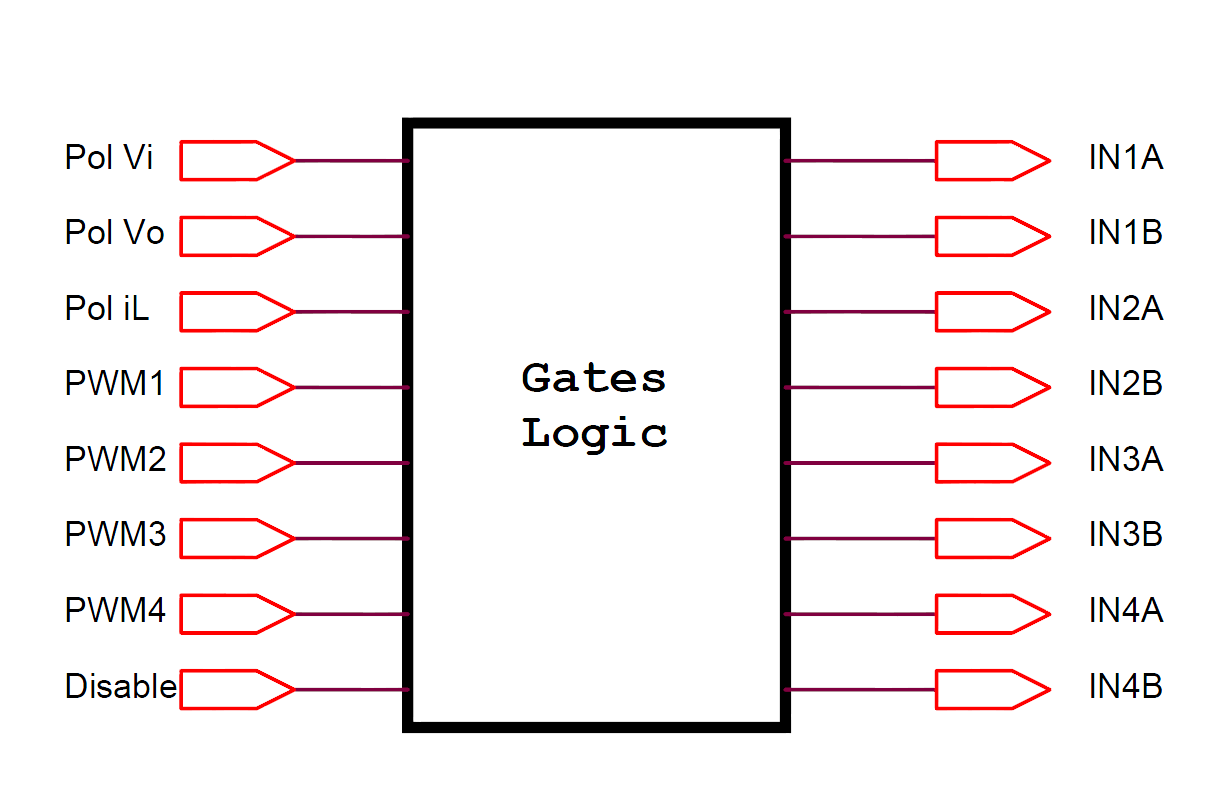


Figure 3 – The gate logic block.

The polarity of voltage detectors is ‘1’ when its sensed voltage > 0 and ‘0’ when sensed voltage < 0. The polarity of the current detector is ‘1’ when the inductor current is flowing from input to output. Input switches S1 and S2 are activated according to input voltage polarity, while S3 and S4 are activated according to output voltage polarity. Figure 4 depicts the configuration of the bidirectional bridge for the four quadrants depending on the input voltage, while Figure 5 depicts the bridge configuration for the four quadrants dependent on the output voltage. A transistor that is always “on” or “off” does not show in the figures. Its series diode is either shown as connected or disconnected. Only pulsed transistors are shown.

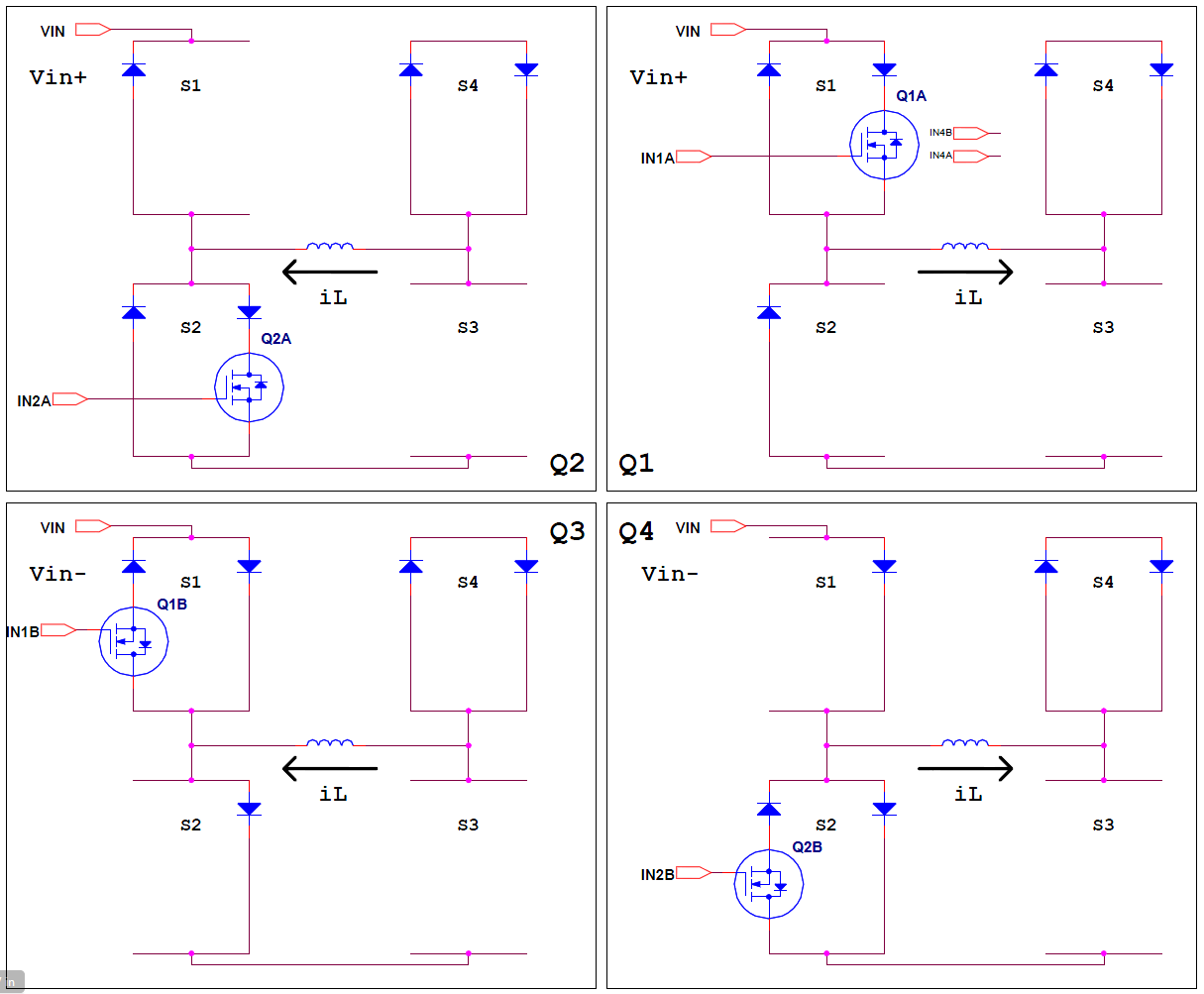


Figure 4 – Buck configuration of the bidirectional bridge for the four quadrants depending on the input voltage. A transistor that is always “on” or “off” does not show in the figures. In the positive half cycle of Vin, the bridge passes between Q1 and Q2 quadrants. While In the negative half cycle, the bridge passes between Q3 and Q4 quadrants.

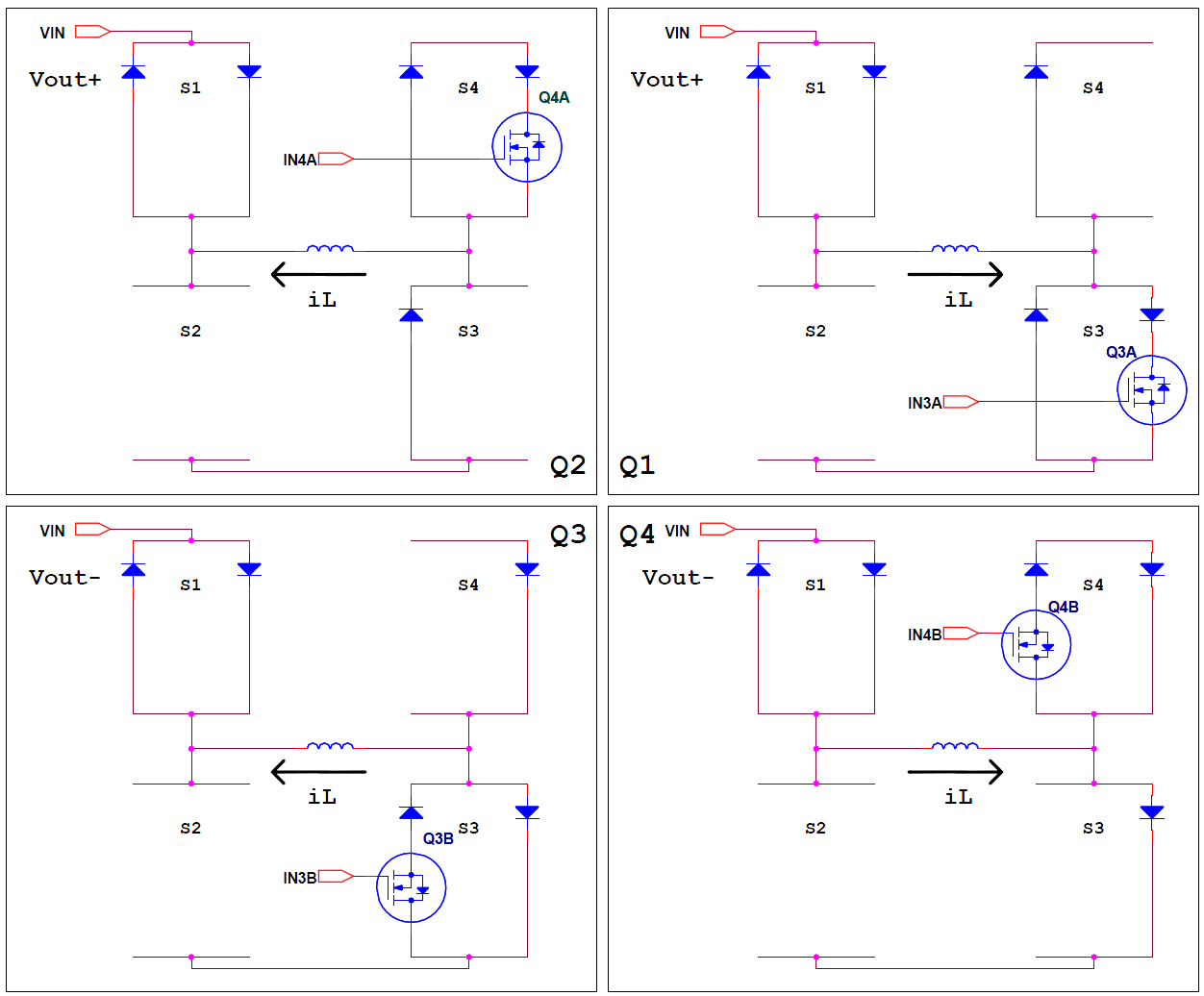


Figure 5 – Boost configuration of the bidirectional bridge for the four quadrants depending on the output voltage. A transistor that is always “on” or “off” does not show in the figures. In the positive half cycle of Vout, the bridge passes between Q1 and Q2 quadrants. While In the negative half cycle, the bridge passes between Q3 and Q4 quadrants.

To implement the digital logic block described in Figures 3-5, we used LCMXO256C Lattice's complex programmable logic device (CPLD) [x1]. The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, control logic, and response time around one ns. These devices bring together the best features of CPLD and FPGA devices on a single chip. Lattice Diamond and VHDL were used to write the CPLD code for simulation and synthesis. Figure 6 depicts the VHDL code that implements the logic control circuit. Using CPLD and VHDL code allows for flexibility in the hardware. One can extend the circuit and change the functionality of the control circuit by software only without modifying the hardware.

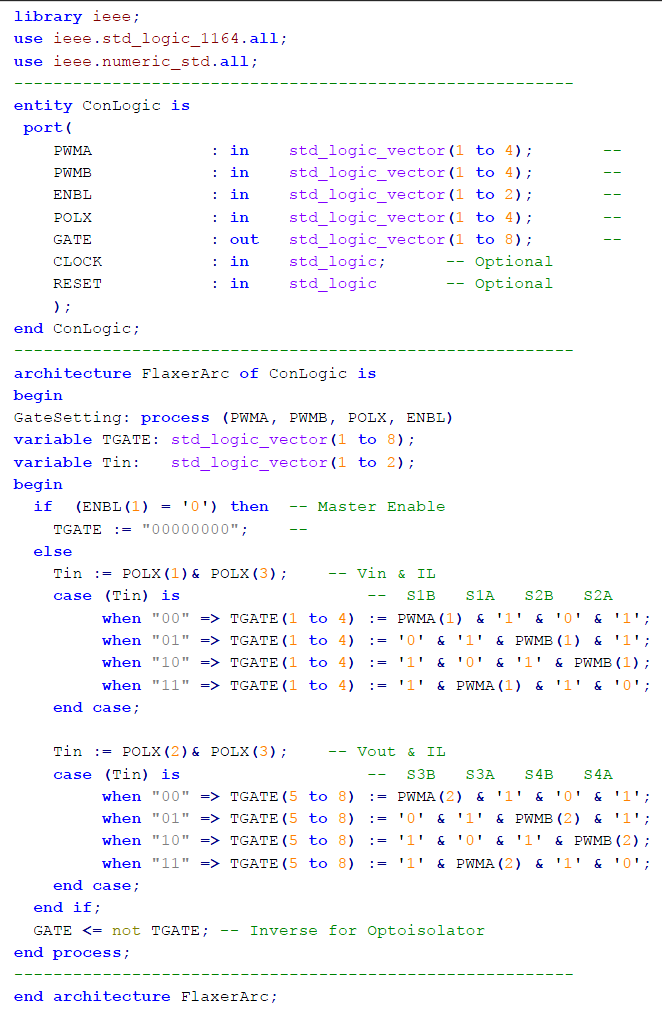


Figure 6 – VHDL code that implements the control logic.

**4. DSP and Embedded Software.**

We have strategically chosen to implement the entire system by real-time embedded software that is running on DSP. The embedded software includes the sampling mechanism, the digital filters, the PID control loop, the PWM timing mechanisms, the polarity detector, communication, and more. Figure 7 describes the block diagram of the embedded software. In order to accomplish all of the above tasks in real-time, we need a suitable high-speed processor with large enough memory. In addition, the processor should contain high-resolution PWM units, 32-bits Timer, and fast ADC units. The most suitable processor for our mission is the Texas Instrument Delfino processor [x2]. This processor currently has several versions running on a clock rate of 150 MHz to 300 MHz. Furthermore, there are versions with multiple cores. In our initial design, we used the TMS320F28335 150 MHz versions (for the new design, TMS320F28377D is preferred). This controller includes a floating-point unit (FPU) essential for real-time calculations of all our tasks, 512 KB of Flash memory for programming and 68 KB of SRAM for the data. It has sixteen fast analog to digital converter (ADC) channels with a conversion time of 80 ns; six enhance capture (ECAP) units that can serve as 32-bits counters, peripheral interrupt expansion (PIE) that supports all peripheral interrupts, and a wide range of communication units (SCI, SPI, CAN, I2C). In particular, this controller includes several channels of enhancing high-resolution pulse width modulation (HREPWM) with a pulse width resolution of 130 ps. The HRPWM unit has a trip zone (TZ) mechanism to give continual protection over the current and short circuit in the load. In addition to the TZ, the microcontroller has a dead band (DB) mechanism designed to drive switches in the full-bridge architecture. We used two complementary HRPWM channels of the DSP (PWM1, PWM2) to trigger the gate driver.

**4.1 Polarity Detector**

Back to Figure 7, the software is based on several interrupts having a well-defined hierarchy. The software's highest priority interrupt is triggered by the PWM mechanism at the bridge's switching rate, which is 150 kHz. The PWM mechanism schedules the ADC unit that generates the interrupt at the end of the conversion. That is, in every PWM cycle that occurs every 6.7 microseconds, the 16 ADC channels are sampled. Three of these 16 channels sample the input voltage (Vin), the output voltage (Vout), and the inductor current (iL). The rest of the ADC channels are sample the input (Ii) and output (Isen) currents and several control values in the system for debugging. The samples of the first three channels (Vin, Vout, iL) are filtered by Median and Finite Impulse Response (FIR) digital filters. The filtered samples are then transferred to polarity detectors that are based on zero-cross detecting. In order to achieve accurate, reliable, and error-free polarity detection, the polarity detector contains a mechanism of hysteresis and a mechanism of blanking. The polarity detectors produce ‘1’ logic in the positive half cycle and ‘0’ in the negative half cycle of each signal. The logic signals are transmitted to the control logic unit mentioned above.

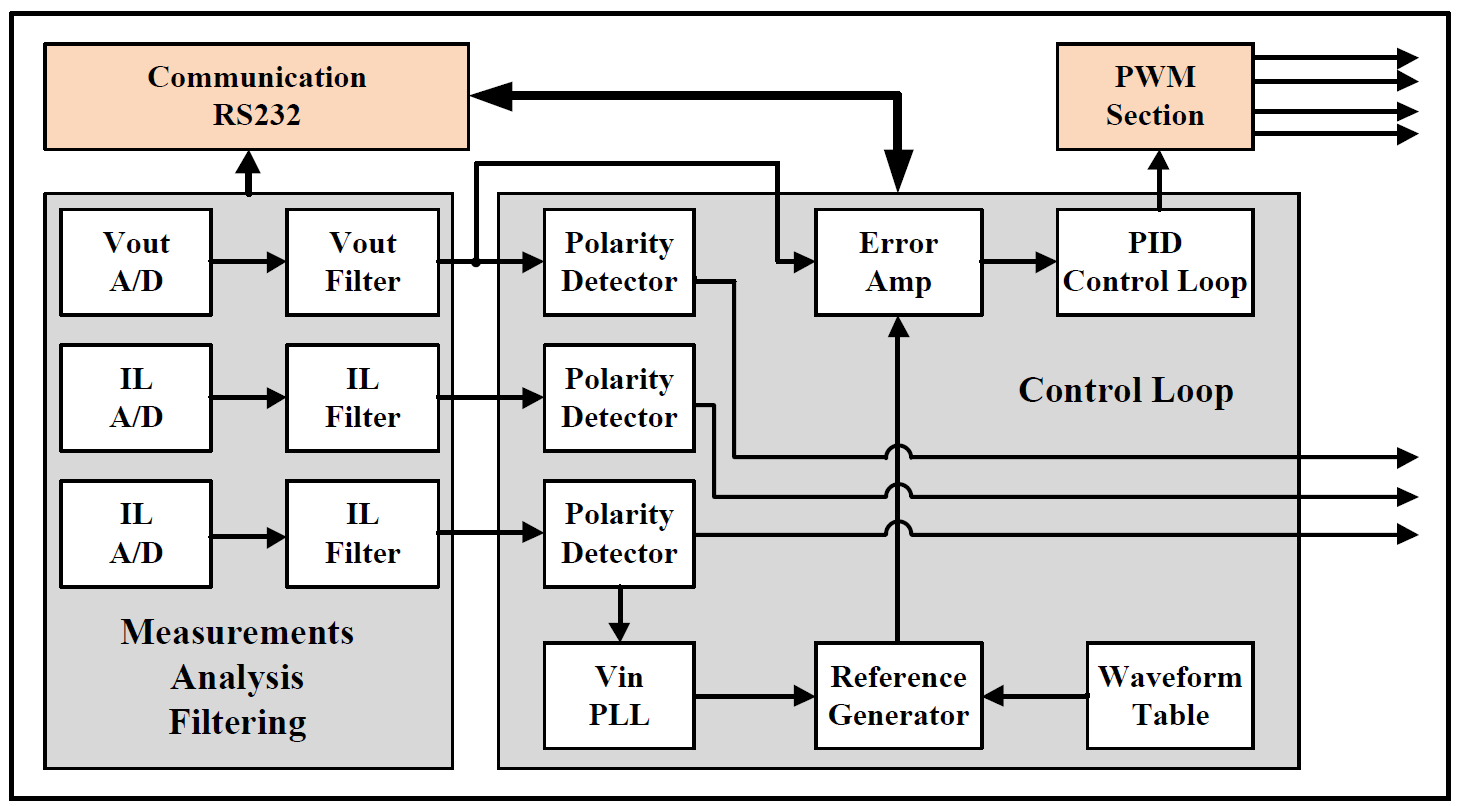


Figure 7 – Block diagram of the embedded software.

**4.2 Reference Generator**

The reference generator produces a unity amplitude sine waveform (or any other selected waveform) with a frequency locked on the input signal (Vin). In order to save real-time calculation time, we calculated the sine values in advance and saved them in a lookup table in the memory. The table contains 256 values (int16 type) of the complete sine cycle. Since we want a 16-bit resolution rather than 8-bit, we performed a real-time linear interpolation between two points in the table.

We use two ECAP unit that contains a 32-bit counter, counting at a rate of 150 MHz, for software implementation of the PLL. One unit (ECAP5) is used as a general-purpose free-running clock in a system with a resolution of 6.7 ns, while the second unit (ECAP1) is used to lock in the input frequency. In addition to polarity, the Vin polarity detector calculates the period (frequency) of the input signal and its phase relative to the output voltage and current. Also, the detector captures the time stamp of the zero-crossing event (from ECAP5).

Using DSP’s TIMER0 unit, we generate two additional lower priority interrupts every 25 us (Int25) and 200 us (Int200). In the Int200 interrupt service routine (ISR), we perform closed-loop control of the ECAP1 period value to lock on the input voltage period time. This process gives us a result where the value of ECAP1 represents the relative time of the input voltage cycle. Using this value, we get the pure mathematical sine value of the synthesized waveform from the lookup table.

**4.3 Closed-Loop Control – PID**

The most significant procedure in the program is the closed-loop control of the output voltage. Remember that our switching rate is 150 kHz, while the input's voltage frequency is 50 to 60 Hz. That is, the control frequency is 2500 to 3000 times greater than the controlled signal frequency. We have used dynamic loop gain to compensate for the alternating nature of the signal, so we can treat the input signal as constant (DC voltage) in the switching frequency time interval. Therefore, at any short time interval, we will treat the converter as a dc to dc converter, considering all the possibilities mentioned earlier. Therefore, the output voltage will be equal to the input voltage multiples by the duty cycle at each short interval. The duty cycle, in our system, is virtually defined as a real number (R) between 0 and 150 percent (0.0-1.5). Since the input voltage and the output voltage are continuously measured at a high rate, the DSP can determine in real-time the working mode in which the converter works - buck or boost; so that the output voltage maintains the expression: Vout = R \* Vin in the entire range of R values. Figure 8 describes the block diagram of the control loop, which includes the transfer functions of all the elements in the loop. The control function gets the instantaneous value of the synthesized waveform F(t), the desired amplitude of output voltage VM, and the peak detection of input voltage VPEAK. The peak value, and the RMS values of the voltages and currents, are calculated continuously in the Int200 ISR.

We can, in this situation, work in an open loop and set the duty cycle to a constant value. In this case, the controller will operate as an unregulated electronic transformer - the output voltage will be a constant product of the input voltage. When working in a closed-loop, one should take into account all the factors that are within the loop, the gain, phase, etc. In figure 8, we can see all of those factors: KADC – is the gain of the analog to digital converter with a reference voltage of 3V and resolution of 12 bits; KDIV – is the attenuation of Vin buffer 1/324; KPWM – is the gain of our PWM unit working in high-resolution mode at a rate of 150 kHz and resolution of 130 ps. The GA block is the relative scale between the synthesized waveform and the Vout. The control’s transfer function - GC is a 2P2Z (2-pole 2-zero) filter reduced to PID control using three coefficients B0, B1, B2. These coefficients are system-specific and not general, so their values need to be optimized.

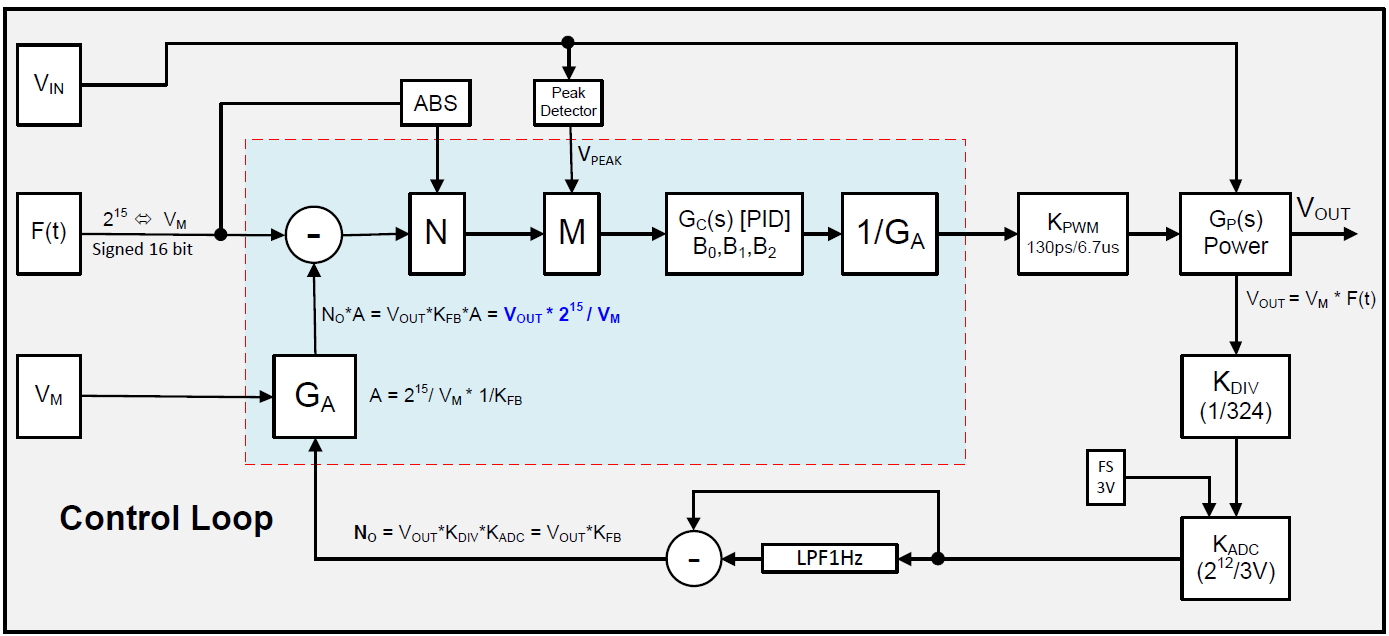


Figure 8 – Block diagram of the closed-loop control.

For VOUT with a given amplitude VM, changes in VIN's amplitude VPEAK change the loop's overall gain. Since we want to keep the loop stable in all conditions, the control process normalizes the overall loop gain by VPEAK to eliminate its influence on the loop response (M unit). In the same way, we have the option to normalize the overall loop gain by F(t) to eliminate its influence on the loop response (N unit). The control loop is running in the Int25 ISR.

**5. Communication Software and User Interface**

To communicate with the converter, a control application was written using C language and the National Instrument [x3] Lab Windows CVI environment. The program running on a PC connects to the microcontroller via the RS-232 port. The application can determine: the desired output voltage (Set Vout), the current limits (Set Current), the control mode (Close-Loop or Manual Open-Loop), the waveform type (Sine or Triangular), the duty cycle for open-loop (Set Duty), turn the controller on/off (Disable, Enable), and the PID coefficients (PID Index). In addition, the application can read the following parameter: input voltage (Vin), frequency (Freq), output voltage (Vout), and duty cycle (Duty). Figure 9 shows the GUI of the control software.

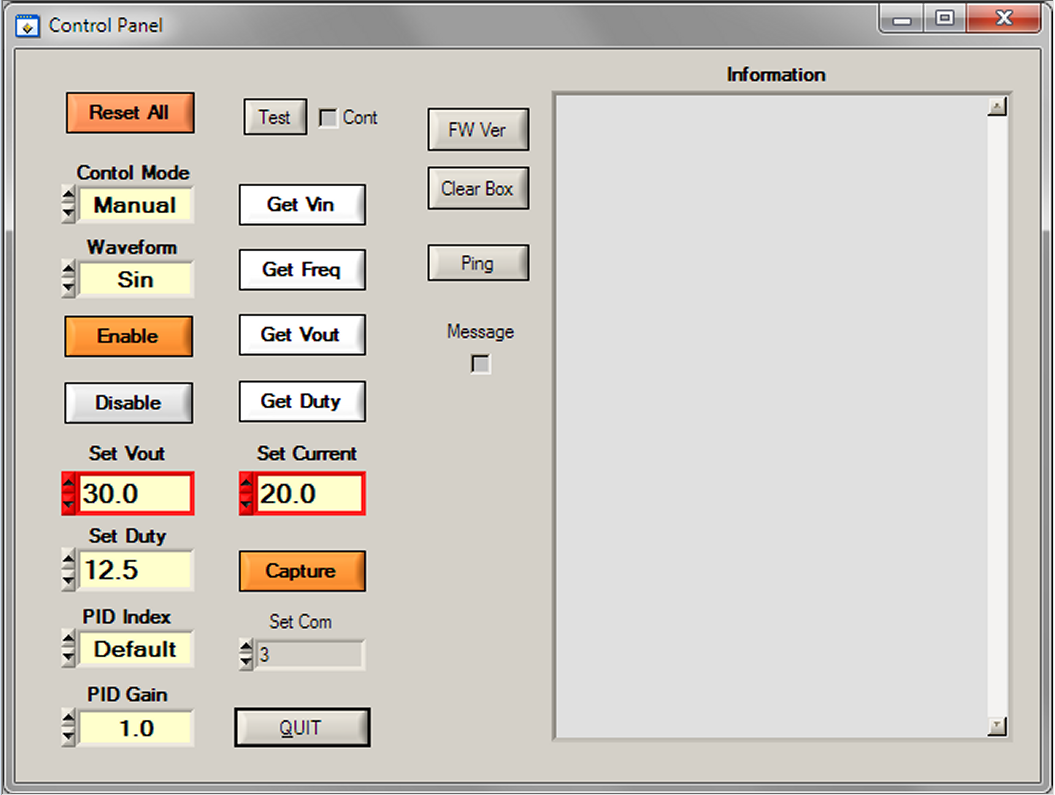


Figure 9 – The software control panel – is used to set and get the overall parameters of the converter.

**6. Electric Circuit**

In order to maintain flexibility, we split the electric circuit into two partial builds on two separate printed circuit boards (PCB). One PCB includes the digital control consisting of the CPU and CPLD, and the second PCB includes the bridge power devices, capacitors, inductors, auxiliary power supply, and other devices. Figure 10 shows the PCB of the digital circuit with all its components, and Figure 11 shows the power PCB.

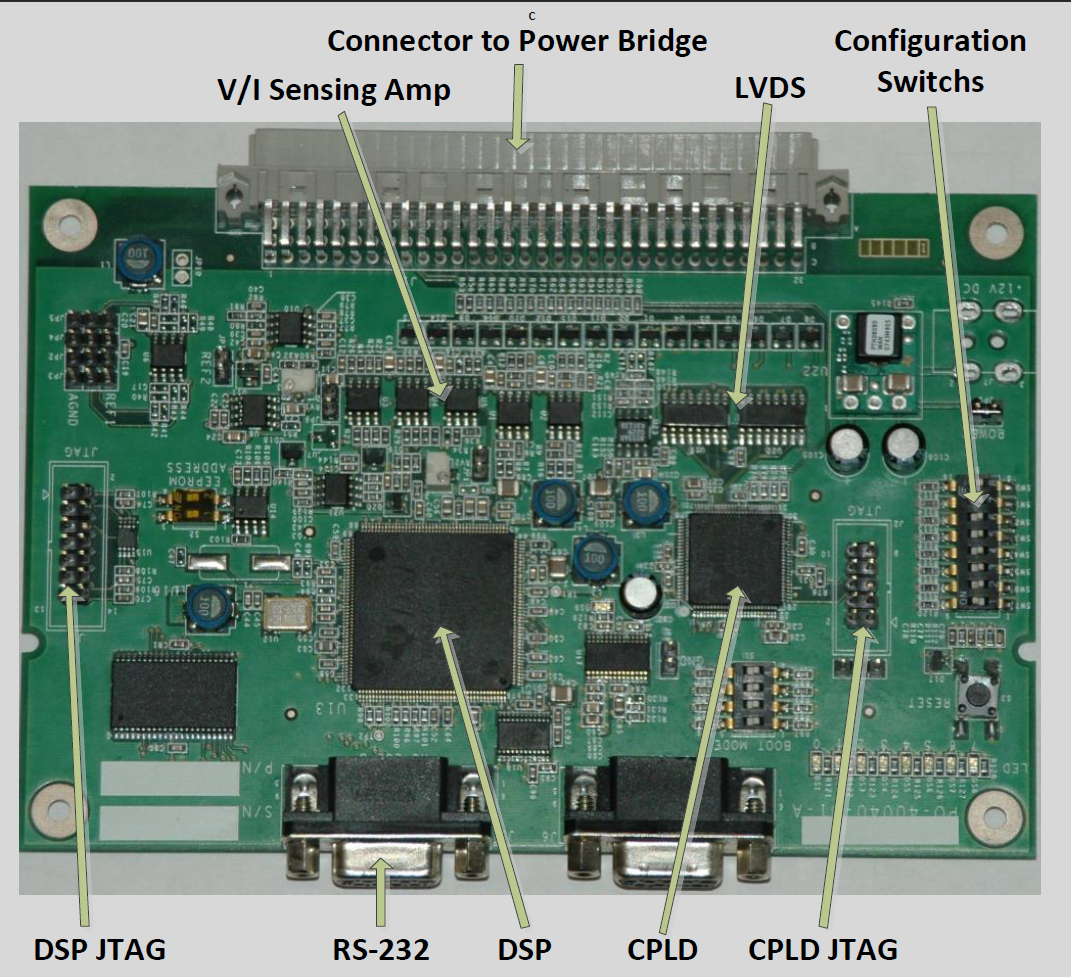


Figure. 10: The PCB of the control unit with all its components. The connector at the top connects to the analog power unit.

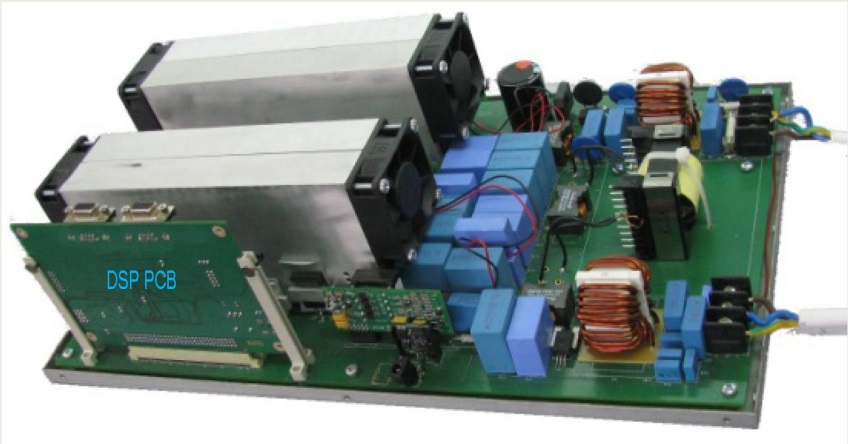


Figure. 11: The power PCB includes the bridge, capacitors, inductors, and auxiliary power supply. On the lower left side, we can see the DSP PCB that was installed on the connector. The dimension of the power PCB is 25x40 cm, and its weight is 2.5 Kg.

**7. Results**

The various system functions were tested to verify the performance and responsiveness of the electronics, and then to evaluate the system’s performance as a regulated electronic transformer. To adjust the input voltage, we used Staco’s 3PN1520B variac [x4]. Our initial tests were to check the operation of each part of the converter and then calibrate the converter’s PID coefficients. We used the control software to set the control mode to a closed-loop, the waveform to sine, and the peak output voltage to 100 volts, while the input peak voltage is around 180 volt and the load is a resistor of 20 ohms.

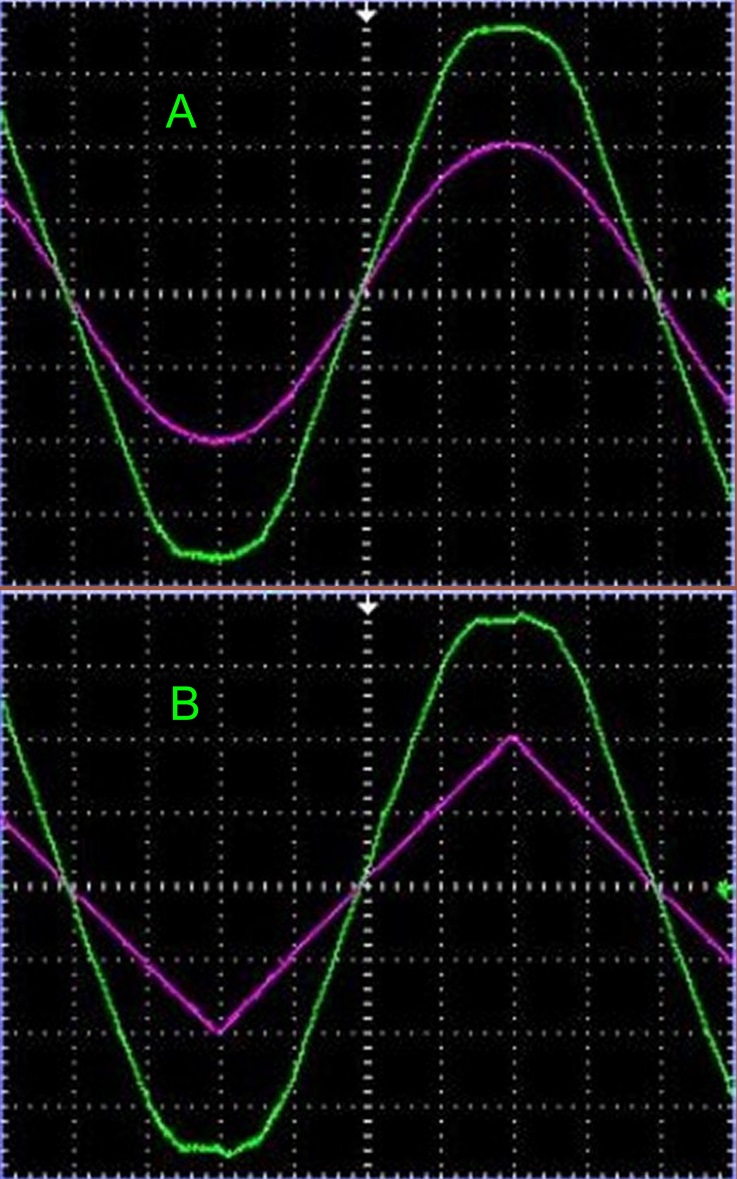
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Figure. 12: The output voltage versus the input voltage for closed-loop mode, the input peak voltage of 180 V, and output peak voltage of 100 V. A) sine waveform, B) Triangular waveform.

After finding the optimal PID coefficients, we measured the output voltage versus the input voltage shown in Figure 12 A. It can be seen that the input voltage is entirely unclean and contains distortions throughout the period. On the other hand, the output voltage shows a clean sinusoidal wave without distortion, locked to the input signal, at a peak voltage of 100 volts as requested. To illustrate the performance of the converter more dramatically, we repeated the experiment when the desired waveform was triangular, shown in Figure 12 B. It can be seen that the input voltage is unclean, while the output voltage shows a clean triangular wave, locked to the input signal, at a peak voltage of 100 volts.

**8. Conclusions**

This work presents an innovative development of direct, stabilized, controlled, and protected AC-AC conversion. We have developed the first electronic transformer based on single AC-AC conversion. The transformer we developed can lock on any voltage (110 V or 220 V) with a frequency between 45 and 65 Hz. The system we show is a single-phase with a power of 4 kilowatts where the efficiency is better than 97%.

**Acknowledgments**

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