RISC-V AND MACHINE LEARNING ACCELERATOR HACKATHON – ENHANCING UNDERGRADUATE STUDENTS’ PERCEPTIONS OF ESSENTIAL CHIP DESIGN SKILLS

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Abstract

The demand for chip design skills has never been as high as it is today. While semiconductor companies struggle to hire skilled students and engineers, the design complexity of VLSI (very large-scale integration) systems is continuously growing. Such technological challenges potentially introduce an entry barrier that prevents many students from expanding their VLSI knowledge and design skills. Furthermore, it has become even more challenging to attract students to this field because of competition from new emerging domains such as data sciences and cyber and mobile applications.

In this paper we present a novel hackathon that aims to deepen undergraduate students’ insight of digital hardware design skills while demonstrating its broader contexts in machine learning computational acceleration. The hackathon theme introduced a design challenge of a machine learning accelerator in conjunction with a RISC-V microprocessor on an FPGA (field-programmable gate array) platform. The hackathon offered the participants a learning environment where they could practice, collaborate with teammates, share innovative ideas, and enhance their soft skills without any formal educational supervision.

As part of the hackathon, an FPGA board was provided to each participant with a reference design as a baseline for the challenge. In addition, a training workshop was conducted which included basic training in operating the FPGA board, designing in Verilog, running the software toolchain, and machine learning basics. All the necessary tools, training workshop recordings, and reference materials were provided online to all hackathon participants.

Through the analysis of the hackathon data, which was performed as a part of this study, we examined students’ perceptions of the required skills prior to the hackathon challenge as well as the day after its completion. A total of 30 students, representing a range of seniority levels at the electrical and computer engineering departments, answered open questionnaires before and after the event. In addition, students were asked to highlight any significant changes in their perceptions following participation in the hackathon. Quantitative and qualitative data extracted from the questionnaires were validated, processed, analysed, and categorized by engineering education experts. According to our findings, while technical know-how and persistence were considered as essential before and after the event, students testified that the event emphasized the importance of additional skills such as team collaboration, system-level thinking, and hardware-software integration

Keywords: hackathon, RISC-V, machine learning, students’ perceptions, electrical engineering, computer engineering

# INTRODUCTION

The modern computing era has fuelled the growing demand for semiconductor integrated circuits (ICs). Today IC chips are the fundamental building elements in many computational systems such as mobile, IoT, desktops, and cloud computing. In the recent years, the semiconductor industry has been struggling to recruit qualified chip design engineers with diverse skills such as logical design, verification, physical design etc. The impact of the shortage of engineers on the semiconductor industry is highly significant as it induces schedule delays and revenue losses. With the advancement of VLSI (very large-scale integration) technology, the design complexity continuously grows, and as a result it may discourage students from intensifying their chip design knowledge and skills. In particular, emerging fields such an artificial intelligence, mobile applications and data science escalate the situation due to their intense competition and attraction.

This paper presents a novel hackathon that intends to intensify undergraduate students’ understanding of digital hardware design skills while demonstrating its larger applications in machine learning computational acceleration. The hackathon challenge called for designing the fastest machine learning accelerator in conjunction with a RISC-V microprocessor [1] on an FPGA (field-programmable gate array) platform. The development environment which was provided to the hackathon participants before the event included the FPGA board, simple RISC-V microprocessor, which was written in Verilog and compiled into the FPGA, a C compiler and a simple C program which ran on the FPGA. All development material was provided with recorded videos and demos in order to facilitate the ramp-up of participants prior to the hackathon event. Without any formal educational supervision, the hackathon provided participants with a learning environment in which they could practice, cooperate with peers, discuss innovative ideas, and improve their soft skills.

Extensive past literature reviews have described hackathons diverse practices and associated vast learning outcomes [2] [3]. The aim of this study is to examine also the change at students’ perception of essential (also referred as ‘soft’) skills required for a successful engagement along the technological challenge both prior and following the hackathon event. Such a change can provide an indication with respect to achieving an ancillary outcome of assimilating those essential skills practice along the challenge.

The rest of the paper is organized as follows: Section 2 describes the hackathon event and the methodology for analyzing the hackathon data. Section 3 present the result of our study and Section 4 summarizes our conclusions.

# METHODOLOGY

## Technical Challenge

The hackathon challenge incorporated multidisciplinary system-level technical skills which combines micro-architecture, chip design, software and machine learning algorithm. The FPGA platform that was used in the hackathon is the Terasic DE0-CV [4] which is illustrated in Figure 1. The platform uses the Altera Cyclone V FPGA device [5] with various peripheral devices such as 7-segment display, LEDs, switch buttons and push buttons. The FPGA platform was provided to every participant in the hackathon.



Figure 1. Terasic DE0-CV FPGA platform (photo credit Terasic Inc.[[1]](#footnote-2)\*)

As part of the FPGA platform a Verilog model of a simple 32-bit integer RISC-V processor was provided. The RISC-V used code memory which stored the binary machine code and a data memory which host the program data. The hackathon participants were required to design the fastest machine learning accelerator which offloaded the RISC-V processor from the matrix multiplication operations. The matrix multiplication accelerator was designed such that was mapped to the memory address space of the processors. The matrices data for the matrix multiplication were store in the processor data memory. This approach allowed the hackathon participants to combine both hardware and software as part of their overall system solution. The Verilog model of both RISC-V processor and the matrix multiplication accelerator were designed using Intel® Quartus® FPGA Design Platform [6] software which was used to simulate and synthesize the design into the FPGA. As part of the development platform, a C compiler was provided for the RISC-V processor. The compiler produced a binary image which was loaded into the processor code memory. A simple “hello world” C code example which toggled the display LEDs, which was provided as part of the development platform, was used to assure that the system was set up and installed correctly. The FPGA block diagram and development environment are illustrated in Figure 2.



Figure 2. FPGA Block Diagram and Development Environment

With respect to the logistical aspects of the hackathon event, the organizing staff created an online registration web site where students could enrol to the hackathon download all the development platform. Every registered team could include up to three students. The web site also included online training videos and the needed material in order to ramp up the participants knowledge to the needed level before the hackathon. In addition, as part of the event preparations, the technical mentors conducted several online zoom meetings where all participants were guided through the installation of the FPGA design environment. All teams were required to run a simple C program to assure that all components were properly operational. Through the hackathon event, mentors from both industry and academia provided an on-going mentoring process. Last, all teams presented their final outcome in front of the hackathon judging committed which chose the top 3 winning teams.

## Assessment of students’ undertaking

Twenty-five students of electrical and computer engineering ranging from junior year up to 4th year senior students, of those participating in the event, took part of the study which comprised of two parts. The first part consisted of a close-ended five-level Likert-like questionnaire which included 20 success factors related to the technical challenge. Students were requested to rank the success factors where 5 indicated that the related factor was highly needed down to 1, not needed at all. The 20 statements reflected three different categories of essential skills:

1. Self-management and persistence, e.g., flexibility and prioritizing skills.
2. Inter-personal and communication, e.g., listening to others, collaboration, presentations skills’ teamwork and presentation skills
3. Technical and engineering thinking, e.g., acquiring both high-level and low-level perception of tasks, embracing multidisciplinary, detecting and mitigating risks

All event participants were required to complete the same questionnaire prior and after the event.

In the second part, an open-ended questionnaire was provided where participants were asked to reflect their opinion with respect to the most needed skills for succeeding in hackathon challenge. The questionnaire was presented to participants twice, prior and following the event. In addition, students were asked to emphasize any change they experienced. In addition, an un-biased observer of the faculty staff, that participated in this part, was asked to report his observations related to participant perception of needed skills.

# Findings

An analysis of students’ answers, has been performed on pre- and post event results, aiming to understand whether the technological challenge altered student view of essential skills.

## Analysis of the open-ended qualitative data

The analysis of the qualitative data allows identifying the shift in views, and its interpretation, as well as the main challenges encountered by the participants. Table 1 reflects a partial sample of students’ feedbacks accompanied by observer interpreter.

Table 1. Major success factors as viewed by a sample of students pre- and post-event

|  |  |  |  |
| --- | --- | --- | --- |
| **Student** | **Prior** | **After** | **Observer interpretation** |
| 1. | *“Technical interest and persistence”*  | *“Teamwork and collaboration…a single person soon reaches a saturation”*  | Acknowledging the limitation of an individual and adopting to teamwork  |
| 2. | *“Identification of the problem and rapid implantation of a unique solution”*  | *“a better preparation was needed …Verilog workshop in particular “* | The task presented the student with a knowledge gap he failed to fill |
| 3. | *“Persistence and knowhow”* | *“Persistence knowhow, self-learning abilities and understating Software-Hardware interfacing”* | The task presented the student with a knowledge gap she partially overcame |
| 4. | -- | “P*rior knowledge, ability to fragment the problem into smaller parts, teamwork and high-level perspective”* | The task presented the student with a knowledge gap she overcame via teamwork and self-paced learning  |

Overall, the finding suggests that most of the teams found the technical hurdle somehow highly challenging to overcome. Some of the students (such as student 2 In Table 1) have chosen not to complete the task, while those who have demonstrated persistence found support through teamwork. Therefore, we conclude that the hackathon challenge has been perceived by the students as highly challenging and demanding.

## Analysis of the statements grading data

The 20 statements, were graded by the students from 1 (not relevant at all) to 5 (very much needed for the hackathon success), producing a maximal final grade of 100. The pre-task calculated grade is 83 while the post-task grade is 85. This observation may suggest that students view of essential skills did not change on average.

### Distinct statements or students

As part of our data analysis, we have examined the answers or every statement in the questionnaire prior and post hackathon event. Similar to the overall grade which did not exhibit a major difference pre-hackathon and post-hackathon, the answers for every statement also exhibited a high-level of similarity. The only meaningful observed deviation was related to the statement “Ability to secure knowledge and technical resources for the project”. The pre-hackathon calculated average was 3.6, while the post event average was 4.6. This observation indicates that the participants mindset has change from a personal task to a wider team challenge. An additional examination of the scoring of every individual student prior and after the event was performed in order to detect anomalies. The results indicate that the majority of the students retained similar final grade (pre and post event), however a minority of students reflected a major change in the success factor final grade. For this observation, it is useful to view the grade of the same students whom their open-ended statements are described in Table 1 as shown in Table 2.

Table 1. Student’s final sum of success factors grades (partial)

|  |  |  |  |
| --- | --- | --- | --- |
| **Student** | **Prior Final Grade** | **After Event Final Grade** | **Notes** |
| 1. | *87*  | *84*  | Similar estimation of essential skill required  |
| 2. | *85*  | *63* |  |
| 3. | *79* | 93 |  |
| 4. | -- | *--* | Did not complete the closed end survey |

The results suggest that the individual estimation of the required essential skill value might have been severely biased following a failure or achieving meaningful success on the technical side. This observation may also suggest that enhancing soft skills perception of engineering students can only be achieved while the technical challenge is well balanced.

### Analysis of statements score by category

While the final essential skills grade was almost the same, a finer look into those skills grades average, is illustrated in Figure 3. The results indicate that the participation in the hackathon event, did not diminish the importance of essential skills as perceived by students. While self-related skills are evaluated the same before and after the event, the “softer” skills such as team work and higher level thinking are intensified due to the hackathon event.



Figure 3. Average Grade on the scale of 1 to 5, of the perceived necessity of essential skills when those are dived into three major categories, before and following the Hackathon event.

# DISCUSSION AND CONCLUSIONS

This paper presents a novel hackathon that aimed to strengthen undergraduate students’ interest in chip design and understanding of hardware design skills. The hackathon offered a unique theme that which included a design of a RISC-V processor in conjunction with a machine learning accelerator on an FPGA board. The hackathon challenge also emphasized the importance of system-level perspective and the importance of software understanding as part of the hardware solution.

The overall feedback granted by the open-ended questions, as well as the perspective of the independent observer, suggest that the students encountered a significant barrier in a 30-hour timeframe of the hackathon. In particular, the need to master an unknown new HDL (Hardware-Description-Language) of the RISC-V processor in a short period has become a major challenge. Looking forward to spring 2022 hackathon event, it is realized that a similar wide gap might appear again. In order to reduce this potential gap, we may consider practicing different strategies such as strengthening the students training process prior to the hackathon. For example, one of the considered options is to provide all participants a preparation environment which will help the teams to deep dive into the development environment in stress-free environment. Another approach suggests enhancing the inter-team collaboration through hackathon that may help the participants leverage insights and lessons learned by their collogues. This can be done via intermediate presentations and exchange of team’s progress reports. Such an approach can be adopted if the hackathon timeframe is extended in similar fashion as done at Ohio State University [7], along adopting other practices, such as having Alumni participants at the event.

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