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CHEN YUAN

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EMPLOYMENT

Research Assistant | **The University of British Columbia** | **Sep. 2015-Present**

Full Duplex Wireline Transceiver

- Implemented and measured a 15Gb/s low-power full-duplex wireline transceiver in 65m CMOS
  (Manuscript submitted to IEEE Journal of Solid-State Circuits in Mar. 2019)

Supply Insensitive Digital Phase-Locked Loop

- Proposed a supply noise insensitive digital-controlled oscillator
- Implemented and measured a bang-bang digital PLL in 65nm CMOS process
  (Manuscript accepted to IEEE Transactions on Circuits and Systems I in Jun. 2019)

Applications Engineer | **Lumerical Inc.** | **Mar. 2017-Sep. 2017**

- Developed software interface to combine Cadence Virtuoso and Lumerical INTERCONNECT
- Facilitated electrical-optical co-simulation in Virtuoso

Research Assistant | **Shanghai Institute of Microsystems and Information Technology** | **Sep. 2012-Aug. 2015**

- Implemented a millimeter wave FMCW radar receiver in 65nm CMOS process
- Designed on-chip passive devices at millimeter wave band

EDUCATION

Vancouver, BC, Canada | **The University of British Columbia** | **Sep. 2015-Present**

- Currently Pursuing Doctor of Philosophy in Electrical Engineering
- Master of Applied Science in Electrical Engineering. GPA: 93.2%, thesis defended in Dec. 2017
- Master Thesis: *Design and analysis of supply noise insensitive digital PLL* (Advised by Prof. Sudip Shekhar).
- Coursework: *IC for Phased-Locked Loops, IC for High-Speed Data Links, RF Integrated Circuits, Mixed-Signal and RF Integrated Circuits and Systems Tests, Analog Integrated Circuits Design, CMOS Design for Silicon Photonics Applications, Architecture for Learning Systems*

Xi'an Shaanxi, China | **Xidian University** | **Aug. 2008-Jun. 2012**

- Bachelor of Engineering in Electronic Science and Technology. GPA: 88.5%.
- Ranking: 1/35.

TECHNICAL EXPERIENCE

Projects

- CMOS millimeter-wave receiver for FMCW radar application (2012-2015) (**Taped-out in UMC 65nm**).
- Analog type-I phased-locked loop (Fall 2015).
- Low power 10Gb/S serial data link transceiver (Fall 2015).
- Wide-band noise-canceling LNA (Spring 2016).
- High gain, high linearity active mixer (Spring 2016).
- Low power low noise wide band LC-VCO (Spring 2016).
- Verification tape-out of analog/digital IOs and ASIC digital design flow for TSMC 65nm CMOS process (Fall 2016) (**Taped-out in TSMC 65nm**).
- Automatic tuning and calibration of mirroring-based filters using silicon in-resonator photoconductive heaters (Fall 2016).
- Supply noise insensitive All-digital PLL for wireline communication (2015-2017) **(Taped-out in TSMC 65nm)**.
- 20Gb/s low-power full-duplex wireline transceiver (2018) **(Taped-out in TSMC 65nm)**.

Skills

- Experience in mixed-signal integrated circuit design and layout from sub-GHz to mm-Wave band
- PCB design experience for high frequency IC measurement.
- Hands-on experience in lab measurement and debug leading to 4 working chips.
- EM simulation experience for chip level and PCB level.
- Programming Languages: C, VHDL, Verilog, Matlab, Java, Skill.
- EDA Tools: Virtuoso, Cadence Spectre, Calibre, ADS, Synopsys Design Compiler, Cadence Encounter, Altium Designer, etc.

AWARDS AND SCHOLARSHIPS

Numerous scholarships for my academic achievement in undergraduate study:

- National Scholarship, twice, top 1% of students in the university.
- Top Scholarship, once, top 0.5%.
- Outstanding Graduate in Class of 2012, top 1%, highest graduate honor.

PUBLICATIONS

- [1] Ma Jianping; Yuan Chen; Tian Tong, "A new rail-to-rail opamp with bulk-driven input stage and interleaved class-AB ouput stage," Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on , Oct. 2014.
- [2] C. Zhao, C. Yuan, X. Sheng, B. Ding, S. Yuan and T. Tian, "A fully integrated single-chip 35GHz FMCW radar transceiver with high bandwidth in 65nm CMOS process," *2015 Asia-Pacific Microwave Conference (APMC)*, Nanjing, 2015, pp. 1-3.
- [3] C. Yuan, S. Shekhar, "*A Supply-Noise-Insensitive Digitally-Controlled Oscillator*", IEEE Transactions on Circuits and Systems I, (accepted).